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VERIFICATION OF TRANSLATION

The undersigned hereby declares that he/she is fluent in both Japanese and English languages and certifies that to the best of his/her knowledge and belief, the attached document is a true and accurate translation of:

The certified copy of Japanese Patent Application No. 2000-101867.

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JAPANESE PATENT APPLICATION NO.2000-101867

[DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] Method and apparatus for defect analysis of semiconductor integrated circuit

[CLAIMS]

[Claim 1]

A method for presuming a defect point of a semiconductor IC (integrated circuit) comprising the steps of:

inputting a test pattern series comprising two or more test patterns to an input/output terminal of a semiconductor IC under test;

measuring a transient power supply current generated of the semiconductor IC under test generated when the test pattern series is input and determining whether the transient current shows abnormality or not;

obtaining a list (defect point list) of points at which a defect can be detected for the test pattern series indicating an abnormality in the transient power supply current; and

presuming a defect point inside the semiconductor IC under test based on the defect point list.

[Claim 2]

The defect analysis method according to claim 1, wherein

the transient power supply current is determined to be abnormal when pulse width of the transient power supply current is over a predetermined value in the step of determining.

[Claim 3]

The defect analysis method according to claim 1, wherein

the transient power supply current is determined to be abnormal when instant value of the transient power supply current at a predetermined time point is over a predetermined value in the step of determining.

[Claim 4]

The defect analysis method according to claim 1, wherein

the transient power supply current is determined to be abnormal when time integral of the transient power supply current is over a predetermined value in the step of determining.

[Claim 5]

The defect analysis method according to any one of claims 1 to 4, wherein

the step of presuming a defect point is a step of presuming a defect point of a semiconductor IC under test included in common for all of the test pattern series where the transient power supply current shows abnormality when the transient power supply current shows abnormality for a plurality of test pattern series.

[Claim 6]

The defect analysis method according to any one of claims 1 to 4, wherein

the step of presuming a defect point is a step of presuming a defect point of the semiconductor IC under test by, based on a defect point list (reference defect point list) for a test pattern series that first shows abnormality in the transient power supply current when the transient power supply current shows abnormality for a plurality of test pattern series, sequentially deleting, from the reference defect point list, defect points not on the defect point list (non-defect points) for one or more following test pattern series showing abnormality in the transient power supply current.

[Claim 7]

The defect analysis method according to any one of claims 1 to 4, further comprising a step of obtaining a defect point list for test pattern series not showing an abnormality in the transient power supply current, wherein

the step of presuming a defect point is a step of presuming a defect point of the semiconductor IC under test by, based on a defect point list (defect point candidate list) for a test pattern series that shows abnormality in the transient power supply current of the semiconductor IC under test, sequentially deleting, from the defect point candidate list, a defect point list (normal point list) for test pattern series showing normalcy in the transient power supply current of the semiconductor IC under test.

[Claim 8]

The defect analysis method according to any one of claims 1 to 7, wherein

the step of obtaining the defect point list is a step of performing a defect simulation for a test pattern series to obtain the defect point list.

[Claim 9]

The defect analysis method according to any one of claims 1 to 8, wherein

the defect point list is a list of defect points in units of basic logic circuits.

[Claim 10]

The defect analysis method according to any one of claims 1 to 8, wherein

the defect point list is a list of defect points in units of signal lines.

[Claim 11]

The defect analysis method according to any one of claims 1 to 8, wherein

the defect point list is a list of defect points in units of signal transmission paths.

[Claim 12]

A defect analysis apparatus for presuming a defect point of a semiconductor IC (integrated circuit) comprising:

a test pattern series input means for inputting a test pattern series comprising two or more test patterns to an input/output terminal of a semiconductor IC under test;

a transient power supply current testing means for measuring a transient power supply current generated of the semiconductor IC under test generated when the test pattern series is input and determining whether the transient current shows abnormality or not;

an abnormal pattern series storage means for storing test pattern series for which the transient power supply current of the semiconductor IC under test shows an abnormality;

a defect point list generating means that obtains a defect point list of defect points for each test pattern series stored in the abnormal pattern series storage means; and

a defect point presuming means for presuming a defect point inside the semiconductor IC under test based on one or more defect point lists acquired from the defect point list generating means.

[Claim 13]

The defect analysis apparatus according to claim 12, wherein the

transient power supply current testing means for determining whether the transient current shows abnormality or not includes:

a current pulse width measuring means for measuring a pulse width of the transient power supply current; and

a defect detecting means for determining the transient power supply current to be abnormal when the pulse width of the transient power supply current measured by the current pulse width measuring means is over a predetermined value.

[Claim 14]

The defect analysis apparatus according to claim 12, wherein the transient power supply current testing means for determining whether the transient current shows abnormality or not includes:

a current instantaneous value measuring means for measuring an instantaneous value of the transient power supply current; and

a defect detecting means for determining the transient power supply current to be abnormal when the instantaneous value of the transient power supply current measured at a prescribed time by the current instantaneous value measuring means is over a predetermined value.

[Claim 15]

The defect analysis apparatus according to claim 12, wherein the transient power supply current testing means for determining whether the transient current shows abnormality or not includes:

a current integrated value measuring means for measuring an integrated value of the transient power supply current; and

a defect detecting means for determining the transient power supply current to be abnormal when the integrated value of the transient power supply current measured by the current integrated value measuring means is over a predetermined value.

[Claim 16]

The defect analysis apparatus according to any one of claims 12 to 15, wherein the defect point presuming means for presuming a defect point includes:

a defect point list storage means for storing a plurality of defect point lists obtained for a plurality of test pattern series stored by the abnormal test pattern series storage means; and

a common defect point presuming means for presuming defect points

in the semiconductor IC under test by presuming defect points included commonly in all of the defect point lists stored by the defect point list storage means.

[Claim 17]

The defect analysis apparatus according to any one of claims 12 to 15, wherein the defect point presuming means for presuming a defect point includes:

a reference defect point list storage section for storing reference defect point lists obtained for a test pattern series that first shows abnormality, from among the test pattern series stored in the abnormal test pattern series storage means; and

a non-defect point deleting section for sequentially deleting, from the reference defect point list, defect points not on the defect point list (non-defect points) for one or more following test pattern series showing abnormality in the transient power supply current.

[Claim 18]

The defect analysis apparatus according to any one of claims 12 to 15, further comprising:

a normal pattern series storage means that stores test pattern series that do not show abnormality in the transient power supply current of the semiconductor IC under test;

an abnormal defect point list storage means that stores a plurality of defect point lists obtained by the defect point presuming means for a plurality of test pattern series showing abnormality in the transient power supply current of the semiconductor IC under test;

a normal defect point list storage means that stores defect point lists obtained by the defect point list generating means for the test pattern series stored by the normal pattern series storage means;

a common defect point presuming means for presuming defect point candidates by presuming defect points included commonly in all of the defect point lists stored by the abnormal defect point list storage means;

a defect point candidate lost storage means for storing defect point candidate lists generated by the common defect point presuming means; and

a normal point deleting means for sequentially deleting, from the defect point candidate list, defect points (normal points) included in

the plurality of defect point lists stored by the normal defect point list storage means.

[Claim 19]

The defect analysis apparatus according to any one of claims 12 to 19, wherein

the defect point list generating means generates the defect point lists by performing a defect simulation for test pattern series input thereto.

[Claim 20]

The defect analysis apparatus according to any one of claims 12 to 19, wherein

the defect point presuming means presumes defect points in units of basic logic circuits.

[Claim 21]

The defect analysis apparatus according to any one of claims 12 to 19, wherein

the defect point presuming means presumes defect points in units of signal lines.

[DOCUMENT] SPECIFICATION

[Technical Field]

[0001]

The present invention relates to a defect analysis method and an analysis apparatus for presuming defect points (defect positions) in a semiconductor integrated circuit having open defects causing delay defects.

[Background Art]

[0002]

Conventional method for defect analysis of semiconductor integrated circuit utilized an electron beam tester, an emission microscope, or a liquid crystal to presume the defect point of the semiconductor IC. The defect analysis of semiconductor IC using an electron beam tester is a method to assume the defect point, such as logical defect, by obtaining a voltage difference between normal circuit and defect circuit. The voltage difference can be obtained while observing, using electron beam tester, voltage contrast image of the tested IC to which an input test pattern is given. This is disclosed, for example, in Japanese Patent Publication No. 5-45423. The defect analysis of semiconductor IC using an emission microscope is a method to assume the current leak position by matching the emission image of the tested IC's wiring pattern with the light image from current leak detected by the photon detector (emission microscope), which can detect extremely dim light of a photon level. It is reported, for example, in Japanese Patent Publication No. 10-4128. The defect analysis of semiconductor IC using a liquid crystal is a method to presume the defect point, such as current leak accompanied with some heat, by observing the optical change of liquid crystal, spread on the surface of the tested IC, elicited by input test pattern. It is reported, for example, in Japanese Patent Publication No. 5-74911.

[0003]

On the other hand, defect analysis using defect simulation is a nondestructive defect analysis method. The defect simulation simulates the output from the output terminal responding to given input test pattern after assuming a defect inside the IC. The results of the simulation

are arranged by matching the input-output logical value with the correspondingly assumed defect, so called, fault dictionary. The defect analysis by the defect simulation is, when the output signal from the output terminal is different from the expected value responding to the input test pattern to the tested IC, performed by matching the input-output logical values from the tested IC with the fault dictionary.

[0004]

In order to work on defects without a logical defect such as short defect or current leak defect, a defect analysis method based on IDDQ defect information of semiconductor IC and the input test pattern, accompanied by IDDQ (quiescent power supply current) test and the defect simulation, is proposed. The defect analysis method accompanied by IDDQ test is disclosed, for example, in the Japanese Patent Publication No. 201486/96.

[0005]

[Problems to be solved by the Invention]

However, the defect analysis methods using the electron beam tester, the emission microscope, and the liquid crystal are costly since these methods requires the semiconductor IC to be opened and chip surface of it exposed. Moreover, multi-layer wiring and large integration of semiconductor IC's render it difficult to assume defect positions.

A defect analysis method with input output signal response and defect simulation can simulate only a defect of which model is stuck on single signal line (0 or 1), so called single-stuck defect (stuck-at-0 or stuck-at-1), but neither a defect stuck on multiple signal line, delay defect, nor defect of short circuit in signal wires. Also, since this defect analysis method assumes the initial defect point after detecting the discrepancy between the output value of IC and the expected value, it cannot guess the defect point of non-logical defects, for example short circuit, where the logic did not goes abnormal even with a defect inside the circuit. Furthermore, although defect points of a delay defect and/or open defect accompanying delay defect can be presumed with programming the defect model for the delay defect in the defect simulation, it is difficult to generate a test pattern for observing effects of the delay defect in the semiconductor IC and to effectively presume the defect point of the delay defect.

[0006]

Furthermore, in the defect analysis accompanied by IDDQ test and defect simulation, since the IDDQ test is a method designed to measure a power current of semiconductor IC in its stable state, it is difficult to assume the defect point altering a delay time of a circuit because of a serious damage on excessive information of the semiconductor IC. Also, because the IDDQ test, since it is primarily applied to short defect, cannot detect open defect and abnormality (parametric defects) of local process parameter (sheet resistance, oxidation etc.) causing a delay defects, it has been a problem that it could not detect the defect position of delay defect, open defect, and parametric defect.

[0007]

Therefore, a defect analysis method is needed that can effectively detect a delay defect and/or open defect and presume the defect point.

The object of the present invention is to provide a method and apparatus which can efficiently presume the defect point of a delay defect and/or open defect in a semiconductor IC, without fabricating the semiconductor IC devices, by evaluating the delay defect and/or open defect using a defect simulation and a transient waveform with a highly visible power supply current such as a transient power supply current or an IDDT.

[0008]

[Means for Solving the Problem]

A method of the present invention is a method for presuming a defect point of a semiconductor IC (integrated circuit) comprising the steps of: inputting a test pattern series comprising two or more test patterns to an input/output terminal of a semiconductor IC under test; measuring a transient power supply current generated of the semiconductor IC under test generated when the test pattern series is input and determining whether the transient current shows abnormality or not; obtaining a list (defect point list) of points at which a defect can be detected for the test pattern series indicating an abnormality in the transient power supply current; and presuming a defect point inside the semiconductor IC under test based on the defect point list.

[0009]

Ths defect analysis method can efficiently presume defect points

of delay defects or open defects in a semiconductor IC without processing a device.

The transient power supply current is desirably determined to be abnormal when pulse width of the transient power supply current is over a predetermined value in the step of determining.

The transient power supply current is desirably determined to be abnormal when instant value of the transient power supply current at a predetermined time point is over a predetermined value in the step of determining.

[0010]

The transient power supply current is desirably determined to be abnormal when time integral of the transient power supply current is over a predetermined value in the step of determining.

The step of presuming a defect point is desirably a step of presuming a defect point of a semiconductor IC under test included in common for all of the test pattern series where the transient power supply current shows abnormality when the transient power supply current shows abnormality for a plurality of test pattern series.

[0011]

The step of presuming a defect point is desirably a step of presuming a defect point of the semiconductor IC under test by, based on a defect point list (reference defect point list) for a test pattern series that first shows abnormality in the transient power supply current when the transient power supply current shows abnormality for a plurality of test pattern series, sequentially deleting, from the reference defect point list, defect points not on the defect point list (non-defect points) for one or more following test pattern series showing abnormality in the transient power supply current.

[0012]

The defect analysis method desirably further comprises a step of obtaining a defect point list for test pattern series not showing an abnormality in the transient power supply current, and the step of presuming a defect point is desirably a step of presuming a defect point of the semiconductor IC under test by, based on a defect point list (defect point candidate list) for a test pattern series that shows abnormality in the transient power supply current of the semiconductor IC under test,

sequentially deleting, from the defect point candidate list, a defect point list (normal point list) for test pattern series showing normalcy in the transient power supply current of the semiconductor IC under test.

[0013]

The step of obtaining the defect point list is a step of performing a defect simulation for a test pattern series or referencing a table of defect point lists showing correspondence of the test pattern series obtained from a defect simulation in advance.

The defect point list is desirably a list of defect points in units of basic logic circuits.

The defect point list is desirably a list of defect points in units of signal lines.

[0014]

The defect point list is desirably a list of defect points in units of signal transmission paths.

A defect analysis apparatus for presuming a defect point of a semiconductor IC (integrated circuit), according to the present invention, comprises: a test pattern series input means for inputting a test pattern series comprising two or more test patterns to an input/output terminal of a semiconductor IC under test; a transient power supply current testing means for measuring a transient power supply current generated of the semiconductor IC under test generated when the test pattern series is input and determining whether the transient current shows abnormality or not; an abnormal pattern series storage means for storing test pattern series for which the transient power supply current of the semiconductor IC under test shows an abnormality; a defect point list generating means that obtains a defect point list of defect points for each test pattern series stored in the abnormal pattern series storage means; and a defect point presuming means for presuming a defect point inside the semiconductor IC under test based on one or more defect point lists acquired from the defect point list generating means.

[0015]

With this configuration, the defect analysis apparatus can efficiently presume defect points of delay defects or open defects in a semiconductor IC without processing a device.

The transient power supply current testing means for determining

whether the transient current shows abnormality or not desirably includes: a current pulse width measuring means for measuring a pulse width of the transient power supply current; and a defect detecting means for determining the transient power supply current to be abnormal when the pulse width of the transient power supply current measured by the current pulse width measuring means is over a predetermined value.

[0016]

The transient power supply current testing means for determining whether the transient current shows abnormality or not desirably includes: a current instantaneous value measuring means for measuring an instantaneous value of the transient power supply current; and a defect detecting means for determining the transient power supply current to be abnormal when the instantaneous value of the transient power supply current measured at a prescribed time by the current instantaneous value measuring means is over a predetermined value.

The transient power supply current testing means for determining whether the transient current shows abnormality or not desirably includes: a current integrated value measuring means for measuring an integrated value of the transient power supply current; and a defect detecting means for determining the transient power supply current to be abnormal when the integrated value of the transient power supply current measured by the current integrated value measuring means is over a predetermined value.

[0017]

The defect point presuming means for presuming a defect point desirably includes: a defect point list storage means for storing a plurality of defect point lists obtained for a plurality of test pattern series stored by the abnormal test pattern series storage means; and a common defect point presuming means for presuming defect points in the semiconductor IC under test by presuming defect points included commonly in all of the defect point lists stored by the defect point list storage means. The defect point presuming means for presuming a defect point desirably includes: a reference defect point list storage section for storing reference defect point lists obtained for a test pattern series that first shows abnormality, from among the test pattern series stored in the abnormal test pattern series storage means; and

a non-defect point deleting section for sequentially deleting, from the reference defect point list, defect points not on the defect point list (non-defect points) for one or more following test pattern series showing abnormality in the transient power supply current.

[0018]

The defect analysis apparatus desirably further comprises: a normal pattern series storage means that stores test pattern series that do not show abnormality in the transient power supply current of the semiconductor IC under test; an abnormal defect point list storage means that stores a plurality of defect point lists obtained by the defect point presuming means for a plurality of test pattern series showing abnormality in the transient power supply current of the semiconductor IC under test; a normal defect point list storage means that stores defect point lists obtained by the defect point list generating means for the test pattern series stored by the normal pattern series storage means; a common defect point presuming means for presuming defect point candidates by presuming defect points included commonly in all of the defect point lists stored by the abnormal defect point list storage means; a defect point candidate lost storage means for storing defect point candidate lists generated by the common defect point presuming means; and a normal point deleting means for sequentially deleting, from the defect point candidate list, defect points (normal points) included in the plurality of defect point lists stored by the normal defect point list storage means.

[0019]

The defect point presuming means desirably presumes defect points in units of basic logic circuits.

The defect point presuming means desirably presumes defect points in units of signal lines.

[0020]

[Operation]

Now, an outline of the present invention is provided using CMOS IC, which is a most conventional semiconductor IC, as an example device.

The power supply current of CMOS IC is a power supply current which is flowed into the CMOS IC, and it is the sum of the currents which flow

in each logic gate composing IC.

Transient power supply current

Fig. 1 shows the transient response of CMOS inverter. The transient response is obtained using a circuit simulator. Fig. 1a shows a response of the output voltage V_{OUT} for the input voltage V_{IN} in a transient state and a response current I_{DD} flowing from the power supply to the CMOS inverter. The current I_{DD} is called as a transient current. When the input IN of the inverter changes from "1" to "0" (Fig. 1b), n-MOS and p-MOS are instantly and almost simultaneously turn on, and a short circuit current I_S flows from the power supply to ground when the input voltage is higher than the threshold voltage of n-MOS and lower than the threshold voltage of p-MOS. At this time, to change the output signal line of the inverter from "0" to "1", the current I_C which charges the parasitic capacitance C_{lcad} connected to the output signal line of the inverter flows from the power supply terminal T_{VD} almost simultaneously with the short circuit current. Thus, when a falling transition occurs in the input of the inverter (it is denoted by the suffix "f"), the transient current I_{Gf} flowed into the inverter is the sum of the short circuit current I_{Sf} and the capacitance charging current I_C.

[0021]

$$I_{Gf} = I_{Sf} + I_C \qquad (1)$$

On the other hand, when the input transits from "0" to "1" (the output changes from "1" to "0") (it is denoted by the suffix "r") (Fig. 1c), the current I_{Gr} flowed into the inverter from the power supply terminal T_{VD} is only the short circuit current I_{Sr} although the capacitance discharging current I_D is generated due to discharging of the parasitic capacitance C_{load} connected to the output signal line. Therefore, the peak of the current is a little bit smaller than that of the transient current I_{Gf} during the falling transient.

[0022]

$$I_{Gr} = I_{Sr} \qquad (2)$$

The transfer characteristic of the CMOS inverter shows the current I_S of triangular pulse form as to the change of the input voltage V_{IN} as shown in Fig. 2a. Therefore, the short circuit current waveform I_{Sr} flowed in the CMOS inverter is approximated to be a triangular pulse "I_S" as shown in Fig. 2b if the input voltage V_{IN} changes as a ramp shape,

when the input of the CMOS inverter has a rising transition. Moreover, the short circuit current waveform I_{Sr} of the CMOS inverter for the first start transition of the input signal shown in Fig. 2b is given as the following equation.

[0023]

$$I_{Sr}=\begin{cases} 0, & t\leqq\dfrac{V_{THN}}{V_{DD}}t_r \\ \dfrac{V_{DD}\cdot I_{Smax}}{(V_{SP}-V_{THN})\cdot t_r}t-\dfrac{V_{THN}\cdot I_{Smax}}{(V_{SP}-V_{THN})}, & \dfrac{V_{THN}}{V_{DD}}t_r<t\leqq\dfrac{V_{SP}}{V_{DD}}t_r \\ \dfrac{V_{DD}\cdot I_{Smax}}{(V_{SP}-V_{DD}+V_{THP})\cdot t_r}t-\dfrac{(V_{DD}-V_{THP})\cdot I_{Smax}}{(V_{SP}-V_{DD}+V_{THP})}, & \dfrac{V_{SP}}{V_{DD}}t_r<t\leqq\dfrac{V_{DD}-V_{THP}}{V_{DD}}t_r \\ 0, & t\geqq\dfrac{V_{DD}-V_{THP}}{V_{DD}}t_r \end{cases} \quad (3)$$

[0024]

Here, I_{Smax} is a maximum value of the transient current (short circuit current) flowed into the CMOS inverter, V_{DD} is a power supply voltage, V_{THN} is a threshold voltage of n-MOS transistor, V_{THP} is a threshold voltage of p-MOS transistor, and t_r is a start transition time of the input signal. V_{THP} is indicated as an absolute value. To make the equation simple, it is possible to set the transition start time of the input voltage V_{IN} as 0 with transition finish time as t_r and input voltage as V_{DD}.

The short circuit current waveform Isf for the falling transition of the input signal may be similarly obtained by the equation (4).

[0025]

$$I_{Sr}=\begin{cases} 0, & t\leqq\dfrac{V_{THN}}{V_{DD}}t_f \\ \dfrac{V_{DD}\cdot I_{Smax}}{(V_{DD}-V_{THN}-V_{SP})\cdot t_f}t-\dfrac{V_{THN}\cdot I_{Smax}}{(V_{DD}-V_{THN}-V_{SP})}, & \dfrac{V_{THN}}{V_{DD}}t_f<t\leqq\dfrac{V_{DD}-V_{SP}}{V_{DD}}t_f \\ \dfrac{V_{DD}\cdot I_{Smax}}{(V_{THN}-V_{SP})\cdot t_f}t-\dfrac{(V_{DD}-V_{THP})\cdot I_{Smax}}{(V_{THN}-V_{SP})}, & \dfrac{V_{DD}-V_{SP}}{V_{DD}}t_f<t\leqq\dfrac{V_{DD}-V_{THN}}{V_{DD}}t_f \\ 0, & t\geqq\dfrac{V_{DD}-V_{THN}}{V_{DD}}t_f \end{cases} \quad (4)$$

[0026]

Here, t_f is a falling transition time of the input signal. The start time of the rising edge of the power supply current, the time of

the maximum value Ismax, and the finish time of the falling transition of this case are indicated in Fig. 2b with parentheses.

Capacitance charging current I_C to the parasitic capacitance C_{load} of the output signal line of the CMOS inverter is shown as the following equation if the voltage change of the output signal line is denoted as $v_{out}(t)$.

[0027]

$$I_C = C_{load} \frac{dv_{out}(t)}{dt} \qquad (5)$$

[0028]

These equations may also be obtained for other logic gates than the inverter.

If it is premised that most of the transient current I_G flowed into a logic gate is the short circuit current, it may be approximated to be a triangular pulse as shown in Fig. 2b. In fact, the form of a transient current I_G of the CMOS inverter is a triangular pulse as shown in Fig. 1a. Therefore, the transient current I_G of a logic gate is monotonously increased until it reaches the maximum value I_{Smax}, and monotonously decreased after the maximum value I_{Smax}. Further, the transient current I_G becomes the maximum value I_{Smax} when the input voltage V_{IN} becomes a switching voltage V_{SP}. In other words, as shown in Fig. 2b, the time when the transient current I_G reaches a peak value is substantially coincides with the transition time of an input to a logic gate. Since a logic gate generally has a delay time, an output transition time is delayed to a predetermined period from the input transition time. In other words, the time when the I_G reaches a peak value leads the output transition time a little bit. In this case, it is possible to consider that the falling edge (falling portion) of the form of the transient current I_G coincides with the output transition time. Further, the pulse width of the transient current I_G of a logic gate is proportional to the transient time of an input voltage.

[0029]

Until now, it is assumed that most of the transient current I_G flowed into the logic gate is the short circuit current. However, the

line delay became predominant than the gate delay because the CMOS fabrication process becomes minute. This means that the ratio of the capacitance current I_C to the output signal line becomes larger than the ratio of the short circuit current I_S for the transient current I_G flowed into the CMOS logic gate if it is assumed that the transition time of the input voltage is constant. Therefore, the time when the transient current waveform becomes peak depends on the ratio of the capacitance current I_C for the short circuit current. When I_C is smaller than I_S, a peak of the transient current waveform I_G corresponds to the peak of I_S. Since the peak of I_S corresponds to the transition time of the input voltage, the peak of I_G precedes the transition time of the logic gate. On the contrary, when I_C is larger than I_S, a peak of the transient current waveform corresponds to the peak of I_C. Since the capacitance current I_C is related to the voltage transition of the output signal line, the peak of I_G is nearly corresponds to the transition time of the output of the logic gate.

[0030]

The CMOS IC shown in Fig. 3a has serially-formed four (4) inverters G1, G2, G3, and G4 illustrated in Fig. 1, and the transient currents I_{G1}, I_{G2}, I_{G3}, and I_{G4} which flow in each of the inverters, respectively, are supplied from a power supply terminal T_{VD}. Therefore, transient power supply current response of the IC is the sum of the transient currents which flow in each of the logic gates as the following equation as shown in Fig. 3b.

[0031]

$$I_{DDT}=\sum_{n=1}^{N} I_{Gn} \qquad (6)$$

[0032]

Here, N is the number of the logic gates switched by the inputted test pattern series and N is 4 (four) for the example of Fig. 3.

As the peak (or the falling edge) of the transient current waveform of the logic gate corresponds to the transition time of the output of the logic gate, the final peak (final falling edge) of the transient current waveform of the CMOS IC corresponds to the output transition time of the logic gate of the CMOS IC which switched last. Therefore,

path delay time of the circuit is obtained by detecting the final peak (final falling edge) of the transient current waveform of the CMOS IC and comparing this to the input transition time. Here, the time of the final peak (final falling edge) of the transient current waveform may be obtained as the maximum value of the time, for example, from the transition time of the input of the path of the IC to the time when the transient power supply current becomes a predetermined current value. The predetermined current value is the value of the power supply current when the output of the final logic gate on the path to be tested becomes the half of the power supply voltage and it may be obtained using circuit simulation for the circuit to be tested or the statistics of the result devices.

[0033]

The delay defect of the path to be tested can be detected by comparing the obtained delay time to the predetermined time (for example, a period TCLK of the system clock).

Delay Defect

First, a delay defect is defined. It is assumed that the path $P=\{g_0, g_1, g_2, \ldots, g_m\}$ is activated utilizing a test pattern series $T=<v_1, v_2>$ (it means that the voltage signal v_1 is followed by the voltage signal v_2) having two test patterns v_1 and v_2. Here, g_0 is the input signal line of path P, and $g_1, g_2, \ldots$, gm are the output signal lines of each of the logic gates $G_1, G_2, \ldots, G_m$ on path P, respectively. At the same time, $g_0, g_1, \ldots, g_{m-1}$ are the input signal lines of each of the logic gates $G_1, G_2, \ldots, G_m$ on path P, respectively. If the signal transition time (the time when the voltage signal is $V_{DD}/2$) of each signal line $g_0, g_1, \ldots, g_m$ is $\tau_0, \tau_1, \ldots, \tau_m$, the gate delay time t_{gdi}, $1 \leq i \leq m$ of each logic gate $G_1, G_2, \ldots, G_m$ on path P is obtained as the following equation.

$$t_{gdi} = \tau_i - \tau_{i-1} \qquad (7)$$

Therefore, a path delay time t_{pc} can be obtained as the sum of the gate delay time t_{gdi} as the following equation.

[0034]

$$t_{pd}=\sum_{i=1}^{m} t_{gdi}=t_m-t_0 \qquad (8)$$

[0035]

However, the actual gate delay time t_{gdi} becomes the value of the following equation because of the effect of the defect.

$$t_{gdi} = t_{gdi,typ} + \delta_i , \quad 1 \leq i \leq m \qquad (9)$$

Here, $t_{gdi, typ}$ is a typical value of the gate delay time of the logic gate G_i, and δ_i is the difference component of the gate delay time. For example, the open defect increases the gate delay time of the only logic gate having defect, and do not increase the gate delay time of the other logic gates. The parametric defect increases the delay times of all logic gates. Path delay time changes as the following equation according to the change of the gate delay time.

[0036]

$$t_{pd}=t_{pd,typ}+\Delta=\sum_{i=1}^{m}(t_{gdi,typ}+d_i) \qquad (10)$$

[0037]

Here, $t_{pd, typ}$ is a typical value of the path delay time of the path P, and Δ is the difference component of the path delay time.

The principle of the delay defect test method is schematically shown in Fig. 4. For the circuit CUT to be tested to operate normally, signal transition generated by the input threshold should be transferred through the path P to be tested to the output threshold in a predetermined time period. Therefore, the path delay time t_{pd} of the path P should satisfy the following condition based on the relation between system clock CLK and between input V_{IN} and output V_{OUT} as shown in Fig. 4b.

[0038]

$$t_{pd}+T_{SU}<T_{CLK}-T_{SKW} \qquad (11)$$

Here, T_{SU} is a setup time of the signal, T_{CLK} is a period of the system clock, and T_{SKW} is a clock skew of the system clock, such as jitter and the ± amount of difference of the edge of the system clock. Equation

(11) may be transformed as the following equation (12).

$$t_{pd} < T_{CLK} - T_{SKW} - T_{SU} \equiv T' \qquad (12)$$

That is, the path delay time t_{pd} of the path P should be smaller than the time T' which subtracts the clock skew or the setup time from the clock period. If t_{pd} is larger than T', the signal transmission through the path P does not correspond to the system clock and the circuit cannot do straight operation. This situation is defined as a delay defect. That is, if t_{pd} is larger than the predetermined time T', it is defined that path P has a delay defect. Here, T' is the maximum value of the permissible delay time.

Open defect (which accompanies a delay defect)

Next, an open defect, which accompanies a delay defect, is defined. An open defect means the electronic discontinuity, which is not intentional, and that one signal line is divided to two or more signal lines. An open defect includes an open contact by the damage of metal or oxide, a metal line open by patterning or etching inferiority, a diffusion layer by the mask inferiority or open of the polysilicon, etc. Moreover, the open defect may be classified as two types. One is an open defect causing a "logic defect" as shown in Fig. 5b, and the other an open defect causing a "delay defect", as shown in Fig. 5. The open defect which accompanying the logic defect makes the logic defect that charging and discharging of the parasitic capacitance accompanied by the signal transition are not conducted and the logic is fixed to the constant value since no current flows on the lines of both sides of the defect if the voltage is applied. On the other hand, if an open defect which accompanying the delay defect is generated, charging and discharging of the parasitic capacitance accompanied by the signal transition are delayed thereby the delay time of the circuit increases since the current amount is smaller than normal although the current flows on the lines of both sides of the defect if the voltage is applied. An open defect which accompanying the delay defect includes a resistive open defect which takes place in the case that the resistance of the signal line becomes larger than the normal value by the defect of the signal line or the resistance between signal lines becomes larger than the normal value by the inferiority of contact, etc., and a minute (<100 nm) open defect that a minute leakage

current flows through the opened signal line by the tunneling effect. For further information on the tunnel current flowing through the minute open defect, please reference C.L. Henderson, J.M. Soden, and C.F. Hawkins, "The Behavior and Testing Implications of CMOS IC Logic Gate Open Circuits," Proceedings of IEEE International Test Conference, pp. 302-310, 1991. In this specification, an open defect which accompanying the delay defect is called as just open defect.

Method for detecting delay defect (using pulse width of the transient power supply current)

Next, a method for detecting delay defect using pulse width of the transient power supply current which is mentioned above is described in detail. This method is to compare the pulse width of the transient power supply current waveform of the circuit to be tested to a predetermined time value. The principle of the method is shown in Fig. 6.

[0039]

It is assumed that a plurality of paths P_1, P_2,..., P_n are activated utilizing a test pattern series $T=<v_1, v_2>$ having two test patterns v_1 and v_2 for the CMOS logic circuit. If τ_{ij} is the time when the jth logic gate from the input of the path Pi switches, the time τmax of the output transition of the logic gate, which switches last, for the paths P_1, P_2,..., P_n is given as the following equation since number of logic gates of each path P_1,..., P_n is different to each other.

[0040]

$$\tau_{max}=\max_{i,j}\{\tau_{ij}\}\ ,\ 1\leqq i\leqq n,\ 1\leqq j \qquad (13)$$

[0041]

Therefore, the maximum value of the path delay time t_{pd}, max for the paths P_1, P_2,..., P_n is the interval between τ_{max} and the time τ_0 of the input transition which is obtained by the following equation.

$$t_{pd,max}=\tau_{max}-\tau_0 \qquad (14)$$

On the other hand, a pulse width t_{PW} of the transient power supply current waveform of the CMOS logic circuit is defined as the time interval between the time τ_0 of the signal transition of the circuit input and

the time τ_{IDD} of the final peak (falling edge) of the transient power supply current.

[0042]

$$t_{PW} \equiv \tau_{IDD} - \tau_0 \qquad (15)$$

As mentioned above, since the time τ_{IDD} of the final peak of the transient power supply current corresponds to the time of the output transition of the logic gate G_{final} which switches last or precedes τ_{max}, the pulse width t_{PW} of the transient power supply current waveform corresponds to the delay time $t_{pd, max}$ of the path P activated by the test pattern T.

$$t_{PW} = \tau_{IDD} - \tau_0 < \tau_{max} - \tau_0 = t_{pd, max} \qquad (16)$$

If, t_{PW} is larger than the maximum value T' of permissible delay time, then it becomes as the following equation.

$$T' < t_{PW} < t_{pd, max} \qquad (17)$$

For the path having the longest delay time $t_{pd, max}$, the transmission of the signal is late to the system clock. That is, the circuit has a delay defect. Therefore, t_{PW} which is larger than T' indicates that there is a delay defect on any side of the activated path, and t_{PW} which is smaller than T' indicates that there is no delay defect in the vicinity of the activated path.

[0043]

No delay defect, $t_{PW} \leq T'$

Delay defect is present, $t_{PW} > T'$ (18)

As described above, a delay defect of a circuit can be tested by comparing the pulse width t_{PW} of the transient power supply current waveform to a predetermined time T'.

Since the transient power supply current of the logic gate decreases monotonously as shown in Fig. 1, the power supply current of the CMOS IC shown in Fig. 3 decreases simply after the output transition time of the logic gate which switches last for the IC. That is, for the CMOS IC without defect, if it is assumed that the output transition time of the logic gate which switches last is τ_{max} and the instant value of the transient power supply current is I', then the transient power supply current of the CMOS IC after τ_{max} may not be larger than I'.

[0044]

Using this principle, a delay defect of the circuit to be test can be detected by measuring the instant value of the transient power supply current of the CMOS IC at a predetermined time point. Here, the current value I' which is the standard for determining a defect is a value of the power supply current when the output of the last logic gate of the path to be tested is a half of the power supply voltage and can be obtained by circuit simulation for the circuit to be tested or the statistics of the result devices.

Method for detecting delay defect (using an instant value of the transient power supply current)

The method for detecting a delay defect using the instant value of the transient power supply current as mentioned above is now described in detail. The method is to measure the instant value of the transient power supply current of the circuit to be tested at a predetermined time point and compare the instant value with the transient power supply current of the golden circuit without delay defect. The principle of the method is illustrated in Fig. 7.

[0045]

It is assumed that a plurality of paths P_1, P_2,..., P_n are activated by the test pattern series $T=<v_1, v_2>$ for the CMOS logic gate. If τ_{ij} is the time when the jth logic gate from the input of the path P_i switches, the time τ_{max} of the output transition of the logic gate, which switches last, for the paths P_1, P_2,..., P_n is given as the following equation.

[0046]

$$\tau_{max}=\max_{i,j}\{\tau_{ij}\}\ ,\ 1\leqq i\leqq n,\ 1\leqq j \qquad (19)$$

[0047]

Therefore, the maximum value of the path delay time $t_{pd,\,max}$ for the paths P_1, P_2,..., P_n is the interval between τ_{max} and the time τ_0 of the input transition which is obtained by the following equation.

$$t_{pd,\,max}=\tau_{max}-\tau_0 \qquad (20)$$

As mentioned before, since the time of the output transition of the logic gate corresponds to the peak or the falling edge, τ_{max} corresponds to the time τ_{IDD} of the final peak or the falling edge of the transient

power supply current waveform I_{DDT}. As the power supply current I_G of the logic gate can be approximated as a triangular wave and G_{final} is the gate switches last, there is no logic gate having a peak of the power supply current after τ_{max}. Therefore, if it is assumed that the time function of the power supply current waveform is $i_{DDT}(t)$, and the instant value of the power supply current at the time τ_{max} is as the following equation,

$$I' \equiv i_{DDT}(\tau_{max}) \quad (21)$$

Then, for t of $t > \tau_{max}$, the following equation is made up.

$$i_{DDT}(t) \leq i_{DDT}(\tau_{max}) = I', \quad t \geq \tau_{max} \quad (22)$$

For normal operation of the circuit, $t_{pd,max}$ should be smaller than the maximum value of the delay time $T'(=T_{CLK} - T_{SKEW} - T_{SU})$.

[0048]

$$t_{pd,max} = \tau_{max} - \tau_0 < T' \quad (23)$$

Therefore, the following equation is made up from the equation (22) at the time point t of $t = T' + \tau_0 > \tau_{max}$ for the circuit without defect.

$$i_{DDT}(T' + \tau_0) < I' \quad (24)$$

If the instant value of I_{DDT} at $T' + \tau_0$ is larger than I', that is, if the following equation is satisfied,

$$i_{DDT}(T' + \tau_0) > I' = i_{DDT}(\tau_{max}) \quad (25)$$

since $T' + \tau_0$ cannot be larger than τ_{max} according to the equation (22), the following equations are made up.

$$\tau_{max} > T' + \tau_0 \quad (26)$$

$$t_{pd,max} = \tau_{max} - \tau_0 > T' \quad (27)$$

For the paths having the longest delay time $t_{pd,max}$, the transmission of the signal is late for the system clock. That is, there is a delay defect in the circuit. Therefore, the fact that the transient power supply current $i_{DDT}(T' + \tau_0)$ at the time $T' + \tau_0$ is larger than I' means that there is a delay defect on any side of the activated path. On the other hand, the fact that $i_{DDT}(T' + \tau_0)$ is smaller than I' means that there is no delay defect in the vicinity of the activated path.

[0049]

No delay defect, $i_{DDT}(T' + \tau_0) < I'$

Delay defect is present, $i_{DDT}(T' + \tau_0) > I'$ (28)

As described above, a delay defect of a circuit can be tested by comparing the instant value of I_{DDT} at a predetermined time with the I_{DDT} level of the circuit without defect.

Integral of the transient power supply current

The time integrals Q_{Sr} and Q_{Sf} of the short circuit currents I_{Sr} and I_{Sf}, respectively, are given as the following equations (29) and (30), respectively, by the equations (3) and (4).

[0050]

$$Q_{Sr}=\int_{-\infty}^{\infty} I_{Sr}dt=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_r$$

$$Q_{Sf}=\int_{-\infty}^{\infty} I_{Sf}dt=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_f$$

(29)、(30)

[0051]

Therefore, the integral QS of the short circuit current flowed in the logic gate during switching is given as the following equation.

[0052]

$$Q_S=\int_{-\infty}^{\infty} I_S dt=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_T \propto t_T \qquad (31)$$

[0053]

Here, t_T is the transition time of the input signal. That is, the integral QS of the short circuit current I_S (I_{Sr} or I_{Sf}) is proportional to the transition time t_T of the input signal. Moreover, Q_S does not depend on the transition direction of the input signal whether it is a rising or a falling transition.

The integral Q_C of the charging current of the output load capacitance C_{load} of the CMOS inverter is given as the following equation from the equation (5) and independent of the input transition time t_T of the CMOS inverter.

[0054]

$$Q_C=\int_{-\infty}^{\infty} I_C dt=\int_{-\infty}^{\infty} C_{load}\frac{dv_{out}(t)}{dt}dt$$

$$=C_{load}\left[V_{OUT}(t)\right]_{-\infty}^{\infty}=C_{load}(V_{DD}-0)=C_{load}V_{DD} \qquad (32)$$

[0055]

Therefore, the integrals Q_{Gf} and Q_{Gr} of the transient currents I_{Gf} and I_{Gr} flowed in the logic gate, respectively, are given as the following equations (33) and (34), respectively, by the equations (1), (2), (31) and (32).

[0056]

$$Q_{Gf}=\int_{-\infty}^{\infty}(I_{Sf}+I_C)dt=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_T+C_{load}V_{DD}\propto t_T$$

$$Q_{Gf}=\int_{-\infty}^{\infty} I_{Sr}dt\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_T\propto t_T$$

(33)、(34)

[0057]

That is, the integral of the transient current of the logic gate is proportional to the input transition time of the logic gate. Fig. 8 shows the result of simulation for the change of the integral of the transient current of the inverter according to the change of the input transition time of the inverter. It can be known that the equations (33) and (34) are right from the Fig. 8.

The CMOS IC shown in Fig. 3a has serially-formed four (4) inverters G1, G2, G3, and G4 illustrated in Fig. 1, and the currents I_{G1}, I_{G2}, I_{G3}, and I_{G4} which flow in each of the inverters, respectively, are supplied from one power supply terminal. Therefore, transient power supply current response I_{DDT} of the IC is the sum of the currents which flow in each of the logic gates as shown in Fig. 3b (the equation (6)). Therefore, the integral Q_{DDT} of the transient power supply current I_{DDT} is the sum of the integrals Q_{Gn} ($1\leq n\leq N$) of the currents which flow in each of the logic gates. N is the number of the logic gates switched by the inputted test pattern series and N is 4 (four) for the example of Fig. 3a.

[0058]

$$Q_{DDT}=\int_{-\infty}^{\infty} I_{DDT}dt=\int_{-\infty}^{\infty}\left(\sum_{n=1}^{N} I_{Gn}\right)dt=\sum_{n=1}^{N}\int_{-\infty}^{\infty} I_{G_{th}}dt=\sum_{n=1}^{N} Q_{Gn} \quad (35)$$

[0059]

In the example illustrated in Fig. 3a, the integral Q_{DDT} of the transient power supply current I_{DDT} is the sum of the integrals Q_{G1}, Q_{G2}, Q_{G3}, and Q_{G4} of the currents which flow in each inverter.

Since the integral Q_{Gn} ($1 \leq n \leq N$) of the current which flows in each of the logic gates is proportional to the input transition time t_{Tn} ($1 \leq n \leq N$) as shown in equation (33) or (34), Q_{DDT} is given as a linear polynominal expression of t_{Tn} ($1 \leq n \leq N$). For example, Q_{DDT} is given as a linear polynominal of the input transition times t_{T1}, t_{T2}, t_{T3} and t_{T4} of the inverters according to the example shown in Fig. 3.

[0060]

$$Q_{DDT}=\sum_{n=1}^{N} Q_{Gn}=\sum_{n-1}^{N} Q_{Sn}+\sum_{n-1}^{N} Q_{Cn}=\sum_{n-1}^{N} a_n t_{Tn}+b \quad (36)$$

[0061]

For the equation (36), a_n is the proportional coefficient between the integral Q_{Sn} of the short circuit current of the logic gate G_n and the input transition time t_{Tn} of the logic gate G_n, and b is an integer term which is the sum of the charging current Q_{Cn} flowed into each of the logic gates.

Open defect (using the integral of the transient power supply current)

Using this principle, an open defect and a delay defect due to the open defect of the path to be tested may be detected.

[0062]

An open defect can be modeled by the large resistance R_{open} because the minute current flows through the defect. Fig. 9a shows an example of a CMOS inverter having an open defect in the input. When the signal transition shown in Fig. 9b is generated on the input signal line A, the signal transition of the signal line A' following the open point becomes late as shown in Fig. 9c. At this time, the signal transition

time t_T of the signal line A' is given as the following equation when R_{open} is the resistance of the open defect and C_{in} is the parasitic capacitance of the input of the inverter.

[0063]

$$t_T = t_{T,typ} + 2.2 R_{open} C_{in} \quad (37)$$

[0064]

Here, $t_{T,typ}$ is the typical value of the transition time of the input signal when there is no defect, and the transition t_T is the time needed to ascend the voltage value from 0.1 V_{DD} to 0.9 V_{DD} (or, descend the voltage value from 0.9 V_{DD} to 0.1 V_{DD}). 2.2 $R_{open}C_{in}$ is the value obtained by $\log_e(0.9\ V_{DD} / 0.1\ V_{DD}) \times R_{open}C_{in}$ when C_{in} changes from 0.1 V_{DD} to 0.9 V_{DD}. That is, the increment of the transition time of the input signal of the inverter is proportional to the resistance R_{open} of the open defect. Therefore, when there is an open defect of the input of the kth inverter on the path to be tested, the integral Q_{DDT} of the power supply of the CMOS IC is obtained by the equation (38) according to the equations (36) and (37), Q_{DDT} changes linearly according to the resistance R_{open} of the open defect, and the increment thereof is proportional to the resistance R_{open} of the open defect.

[0065]

$$Q_{DDT} = \sum_{n=1}^{N} a_n T_{Tn} + b = \left(\sum_{n-1}^{N} a_n t_{nTYP} + b \right) + 2.2 a_k C_{in} R_{open}$$

$$= Q_{DDT,typ} + 2.2 a_k C_{in} R_{open} \propto R_{open} \quad (38)$$

[0066]

Here, $Q_{DDT,typ}$ is the typical value of the integral of the power supply current when there is no defect. 2.2 $a_k C_{in}$ R_{open} of the second term of the right side of the equation (38) is an additional amount according to the input open defect of the kth inverter. This equation (38) corresponds to the result of simulation of the change of Q_{DDT} for R_{open}. Fig. 10 plots the change of Q_{DDT} for the resistance R_{open} of the open defect when there is an open defect on inverter IN2 for the circuit shown in Fig. 3.

[0067]

Therefore, an open defect present on the input end of the logic

gate on the test path can be tested by measuring the integral Q_{DDT} of the transient power supply current and comparing it to the integral $Q_{DDT, typ}$ of the transient power supply current of the circuit without defect. According to the actual CMOS fabrication process, the integral of the transient power supply current changes in the range of $Q_{DDT, typ} \pm \Delta_Q$ due to the difference of the process parameter as shown in Fig. 11. Here, Δ_Q is the change amount of the integral of the transient power supply current. Therefore, when Q_{DDT} is larger than the maximum value $Q_{DDT, typ} + \Delta_Q$ of the integral of the transient power supply current which can be generated in the circuit without defect, it is possible to determine that there is an open defect on the test path. That is, Q_{DDT} which is smaller than $Q_{DDT, typ} + \Delta_Q$ indicates that there is no open defect in the CMOS IC, and Q_{DDT} which is larger than $Q_{DDT, typ} + \Delta_Q$ indicates that there is an open defect in the CMOS IC.

[0068]

No open defect, $Q_{DDT} < Q_{DDT, typ} + \Delta_Q$

Open defect is present, $Q_{DDT} > Q_{DDT, typ} + \Delta_Q$ (39)

Here, $Q_{DDT, typ}$ and Δ_Q can be obtained by the simulation for the process change.

Method for detecting a delay defect (using the integral of the transient power supply current)

Next, a method for detecting a delay defect using the integral of the transient power supply current as mentioned above is described in detail. This method is to evaluate a delay defect by measuring the integral of the transient power supply current of the test circuit and comparing it to a predetermined value.

[0069]

The gate delay time t_{gd} of the logic gate is proportional to the transition time t_T of the input signal as shown in equation (40). (Neil H.E. Weele, "Principles of CMOS VLSI Design-A Systems Perspective" Second Edition, Addison-Weely Publishing Company 1999, pp. 216-217, Sections 4.52 and 4.53).

[0070]

$$t_{gd}=t_{gd,step}+\frac{1}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)t_T \qquad (40)$$

[0071]

Here, $t_{gd,\ step}$ is the delay time of the step input of transition time 0 of the inverter without defect. V_{TH} is a threshold voltage of p−MOS or n−MOS, and $V_{TH} = V_{THN}$ for the rising edge of the input and $V_{TH} = V_{THP}$ for the falling edge of the input. Therefore, gate delay time t_{gd} of the logic gate having an open defect which can be modeled by the resistance R_{open} on the input signal line is obtained by the following equation by substituting the equation (37) to the equation (40) since the input transition time of the logic gate is given as the equation (37).

[0072]

$$\begin{aligned} t_{gd}&=t_{gd,step}+\frac{t_T}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)\\ &=t_{gd,\ step}+\frac{t_{T,typ}+2.2R_{open}C_{in}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)\\ &=t_{gd,\ step}+\frac{t_{T,\ typ}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)+\frac{2.2C_{in}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)R_{open}\\ &=t_{gd,\ step}+\frac{2.2C_{in}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)R_{open}\propto R_{open} \end{aligned} \qquad (41)$$

[0073]

Here, $t_{gd,\ typ}$ is a typical value of the gate delay time of the logic gate without defect. That is, the gate delay time t_{gd} changes by the resistance R_{open} of the defect, and the increment δ of the gate delay time is proportional to the resistance R_{open} of the defect. Therefore, when there are open defects on some logic gates on the test path, path delay time t_{pd} is also proportional to R_{open}. This can be expressed in equation (42) by substituting the equation (41) to the equation (10).

[0074]

$$t_{pd}=\sum_{i=1}^{m} t_{gdi}$$

$$=\sum_{i=1}^{m} t_{gdi,typ}+\frac{2.2C_{ink}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)R_{open}$$

$$=t_{pd,typ}+\frac{2.2C_{ink}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)R_{open}\propto R_{open} \qquad (42)$$

[0075]

This corresponds to the simulation result of the change of t_{pd} for R_{open} as shown in Fig. 12. Fig. 12 plots the change of t_{pd} for the resistance R_{open} of the open defect when there is an open defect on input signal line of the inverter G2 for the circuit shown in Fig. 3a.

The integral Q_{Sk} of the short circuit current of G_k, when there is an open defect on the input of the logic gate G_k on the path P, is given as the following equation from the equations (31) and (37).

[0076]

$$Q_{Sk}=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_{Tk}$$

$$=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}(t_{T,typ}+2.2R_{open}C_{ink})$$

$$=\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}t_{T,typ}+\frac{I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{2V_{DD}}2.2R_{open}C_{ink}$$

$$=Q_{sk,typ}+\frac{2.2I_{Smax}(V_{DD}-V_{THN}-V_{THP})C_{ink}}{2V_{DD}}R_{open}$$

Therefore, the integral Q_{DDT} of the transient power supply current

of the IC becomes as the following equation, and it is also proportional to the resistance R_{open} of the open defect.

[0077]

$$Q_{DDT}=\sum_{n=1}^{N} Q_{Gn}$$

$$=\sum_{n=1}^{N} Q_{Sn}+\sum_{n=1}^{N} Q_{Cn}$$

$$=\sum_{n\neq k} Q_{Sn,\,typ}+Q_{Sk,\,typ}+\frac{2.2I_{Smax}(V_{DD}-V_{THN}-V_{THP})C_{ink}}{2V_{DD}}R_{open}+\sum_{n=1}^{N} Q_{Cn}$$

$$=\sum_{n=1}^{N} Q_{Sn,\,typ}+\sum_{n=1}^{N} Q_{Cn}+\frac{2.2I_{Smax}(V_{DD}-V_{THN}-V_{THP})C_{ink}}{2V_{DD}}R_{open}$$

$$=Q_{DDT,\,typ}+\frac{2.2I_{Smax}(V_{DD}-V_{THN}-V_{THP})C_{ink}}{2V_{DD}}R_{open}$$

(43)

[0078]

Therefore, according to the equations (42) and (43), the delay time t_{pd} of the path P having an open defect changes linearly to the integral Q_{DDT} of the transient power supply current of the CMOS IC. This corresponds to the simulation result of the change of t_{pd} for Q_{DDT} as shown in Fig. 13. Fig. 13 plots the change of t_{pd} for the integral Q_{DDT} of the transient power supply current when there is an open defect on input signal line of the inverter IN2 for the circuit shown in Fig. 3.

The equation (44) is obtained by substituting R_{open} obtained from the equation (43) to the equation (42).

[0079]

$$t_{pd}=t_{pd,typ}+\frac{2.2C_{ink}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)R_{open}$$
$$=t_{pd,typ}+\frac{2.2C_{ink}}{6}\left(1-2\frac{V_{TH}}{V_{DD}}\right)\frac{(Q_{DDT}-Q_{DDT,typ})\cdot 2V_{DD}}{2.2I_{Smax}(V_{DD}-V_{THN}-V_{THP})C_{ink}}$$
$$=t_{pd,typ}+\frac{V_{DD}-2V_{TH}}{3I_{Smax}(V_{DD}-V_{THN}-V_{THP})}(Q_{DDT}-Q_{DDT,type}) \quad (44)$$

[0080]

If the integral Q_{max} of the transient power supply current when the path delay time t_{pd} is the maximum permissible value T', Q_{max} is obtained as the following equation when $t_{pd}=T'$, $Q_{DDT}=Q_{max}$ for the equation (44).

[0081]

$$Q_{max}=Q_{DDT,typ}+\frac{3I_{Smax}(V_{DD}-V_{THN}-V_{THP})}{V_{DD}-2V_{TH}}(T'-t_{pd,typ}) \quad (45)$$

[0082]

Q_{max} is the maximum value of the integral Q_{DDT} of the transient power supply current of the CMOS IC having no open defect. That is, it can be determined that there is no delay defect when Q_{DDT} is smaller than Q_{max}, and the delay defect due to the open defect is present when Q_{DDT} is larger than Q_{max}.

No delay defect, $Q_{DDT} \leq Q_{max}$

Delay defect is present, $Q_{DDT} > Q_{max}$ (46)

As described above, a delay defect of a circuit can be tested by comparing the integral Q_{DDT} of the transient power supply current pulse to a predetermined value Qmax. The predetermined value Q_{max} can be obtained by circuit simulation or the statistics using the equation (45).

[0083]

The transient power supply current is the transient current which flows in the power supply pin of the IC, and it can be observed more easily than the voltage signal. Therefore, the delay defect test method using transient power supply current is superior to the delay defect test method using transient power supply voltage for the function of

detecting delay defects. For example, the delay defect test method using transient power supply voltage can only detect the delay defect if the voltage signal is transmitted to the output signal line of the IC, while the delay defect test method using transient power supply current can detect the delay defect if the voltage signal in not transmitted to the output signal line of the IC because the transient power supply current signal having a pulse width corresponding to the delay time of transmitted path can be observed. Moreover, the delay defect test method using transient power supply current has less limitations for test pattern generation than the delay defect test method using transient power supply voltage because there is no need to transmit to the output signal line for the voltage signal. Therefore, the test pattern can be generated easily. For an extreme case, if the test pattern series is selected at random, it is possible to detect the delay defect of the path activated by the selected test pattern series using the delay defect test method using transient power supply current.

Characteristics of the delay defect test using transient power supply current

Next, a method for generating defect list is explained. Fig. 14 illustrates an example CMOS IC to be tested. This IC has three (3) input terminals I1, I2 and I3, two (2) output terminals O1 and O2, three (3) internal signal node N1, N2 and N3 , and five (5) logic gates G1, G2, G3, G4 and G5. The input terminal I1 is connected to the input of the inverter logic gate G1, the output terminal thereof is connected to one of the input side of NAND logic gate G3 through the node N1, the input terminals I2 and I3 are connected to the input side of the NAND logic gate G2, the output terminal thereof is connected to one of the input side of logic gate G3 through the node N2, the output terminal thereof is connected to one of the input side of the NOR logic gate G5 and the input side of the inverter logic gate G4 through the node N3, the input terminal I3 is connected to one of the input side of logic gate G5, and the output terminals O1 and O2 are connected to each of the output sides of the logic gates G4 and G5, respectively. Moreover, the logic gates G1, G2, G3, G4 and G5 are connected to a common power supply terminal.

[0084]

An example of the defect simulation result conducted on the above CMOS IC to be tested is shown in Fig. 15. In Fig. 15, the first column indicates the identifier(s) of the test pattern series. The second column of Fig. 15 illustrates the input signals (test pattern series) applied to the input terminals I1, I2 and I3 of the CMOS IC, the third column shows the signals generated on the internal signal nodes N1, N2 and N3 of the CMOS IC without defect when each test pattern series is applied, and the fourth column shows the signals generated on the output terminals O1 and O2 of the CMOS IC without defect when each test pattern series is applied. Here, signals "0", "1", "R" and "F" of the second to the fourth columns of Fig. 15 indicate each of the signals <"0", "0"> (the first element in <> is the start signal value and the second elecment is the final signal value) which is always low,), <"1", "1"> which is always high, <"0", "1"> which is a rising signal from low level to high level, and <"1", "0"> which is a falling signal from high level to low level, respectively. Therefore, each test pattern series is composed of two test patterns, for example , the test pattern series T1="00 R" means I1, I2, I3=<"000","001">. That is "000" and "001" are test patterns, and the columns of "000" and "001" are test pattern series. The fifth column of Fig. 15 shows the set of the defect logic gate (defect points list) detectable by the test using transient power supply current when each test pattern series is applied.

[0085]

When a logic gate has a delay defect or an open defect, the transient power supply current becomes abnormal because the switching operation is delayed and thus the transient power supply current waveform changes. Therefore, whether the logic gate which switches by the input test pattern series has a defect or not can be determined by applying the test pattern series and measuring the transient power supply current whether it is abnormal or not. For example, if the test pattern series T2 is applied to the CMOS IC shown in Fig. 14, transition signals are generated on the internal signal node (signal line) N2 and N3 and the output terminals O1 and O2 by the switching operation of the logic gates G2, G3, G4 and G5, whose logic states are shown in Fig. 14, in the CMOS IC to be tested. Therefore, when there is a defect on any of the logic gates G2, G3, G4 and G5, the abnormality of the transient power supply current is detected

by the transient power supply current test having test pattern series T2. Thus, a defect of logic gates of G2, G3 , G4 and G5 can be detected by the transient power supply current test having test pattern series T2. Then, a defect points list for the test pattern series (a list of the gates that the defect is detectable) T2 is obtained as GT2= {G2, G3 , G4, G5} by the defect simulation as described above.

Method of presuming a defect point (logic gate)

Next, a method of presuming a defect point is described in detail. For example, it is considered that the transient power supply current shows abnormality for all the test pattern series when the test pattern series T2, T4 and T6 is applied to the CMOS IC to be tested shown in Fig. 14. According to the result of the defect simulation, a set of the defective logic gates, i.e. a defect points list detectable by each of the test pattern series T2, T4 and T6 is GT2= {G2, G3, G4, G5} , GT4= {G2} and GT6= {G2, G3, G4} , respectively. Therefore, the presumed logic gate to be defective is the common element of the defect points lists GT2, GT4 and GT6, i.e. the intersection of the sets GT2, GT4 and GT6.

$$GT2 \cap GT4 \cap GT6 = \{G2\} \qquad (47)$$

Therefore, the defective logic gate is presumed to be G2.

[0086]

Moreover, the defective logic gate G2 can be presumed by excluding the points (non-defect point) which are not included in the defect points lists GT6 and GT4 from the defect points list GT2 = {G2, G3, G4, G5} of the test pattern series T2 which is set to the standard defect points list. 6. The defect points list that the abnormality of the transient power supply current is detected first is set as the standard defect points list as the following.

[0087]

{G2, G3, G4, G5}

Next, the non-defect points {G1, G5} which are not included in the defect points lists GT6 which generated next are excluded from the standard defect points list GT2. Here, the list of the non-defect points is indicated as the complementary set of the defect points list GT6 (it is denoted by ~GT6). Therefore, the standard defect points list becomes as following

by excluding G5.

{G2, G3, G4}

That is, the only elements which correspond GT6 among GT2 are remained. Then, the non-defect points ~GT4= {G1, G3, G4, G5} G1, G5} which are not included in the defect points lists GT4 are similarly excluded from the standard defect points list. Then, the standard defect points list becomes as following.

{G2}

Therefore, the defective logic gate is presumed to be G2.

[0088]

Next, it is assumed that the transient power supply current shows abnormality when the test pattern series T10 is applied and the transient power supply current is normal when the test pattern series T6 is applied to the CMOS IC to be tested shown in Fig. 14. Here, T10 is called as abnormal test pattern series, T6 as normal test pattern series. According to the result of the defect simulation, a set of the defective logic gates, i.e. a defect points list detectable by each of the test pattern series T10 and T6 is GT10= {G1, G3, G4} and GT6= {G2, G3, G4} , respectively. Here, the defect points included in the defect points list GT6 is called as the normal points. That is, the defective logic gate is any one of the logic gates in the defect points list GT10, and not the and not the ones in the defect points list GT6. Therefore, the presumed logic gate to be defective is present as the intersection of the set GT10 and the complementary set of GT6.

$$GT10 \cap \sim GT6 = \{G1, G3, G4\} \cap \{G1, G5\} = \{G1\} \quad (48)$$

Then, the defective logic gate is presumed to be G1. The method as described above is equivalent to the method of excluding the non-defect points included in the defect points list GT6 from the defect points list GT10.

[0089]

As described above, the defective point can be presumed in terms of the logic gate. However, the present invention is not limited to presume the defect point in terms of the logic gate, it is possible to presume the defect point in terms of the signal line by the defect simulation

on the assumption that the defection is present on the signal line in the IC.

Method of generating a defect point (signal line)

Fig. 16 illustrates an example CMOS IC to be tested. This IC has three (3) input terminals I1, I2 and I3, two (2) output terminals O1 and O2, five (5) logic gates G1, G2, G3, G4 and G5, and twelve (12) signal lines L1, L2,..., L12. Here, the signal lines include input/output signal lines and the branch signal line is denoted as the separate signal line. The output signal lines L11 and L12 are connected to the output buffer G6 and G7, respectively. The input terminal I1 is connected to the input side of the inverter logic gate G1 through the signal line L1, each of the input terminals I2 and I3 is connected to the input side of the NAND logic gate G2 through each of the signal lines L2, L3 and L4 , respectively, each of the output sides of the logic gates G1 and G2 is connected to the input side of the NAND logic gate G3 through each of the signal lines L6 and L7, respectively, the output side of the logic gate G3 is connected to the input side of the inverter logic gate G4 through the signal lines L8 and L9 and to one of the input side of the NOR logic gate G5 through the signal lines L8 and L10, the input terminal I3 is connected to one of the input side of the logic gate G5 through the signal lines L3 and L5, the output side of the logic gate G4 is connected to the output terminal O1 through the signal line L11 and the buffer G6, and the output side of the logic gate G5 is connected to the output terminal O2 through the signal line L12 and the buffer G7. Though it is not shown in the figure, the power supply terminals of the logic gates G1, G2, G3, G4 and G5 and the output buffers G6 and G7 are connected to a common power supply.

[0090]

An example of the defect simulation result conducted on the above CMOS IC to be tested is shown in In Fig. 17, the first column indicates the identifier(s) of the test pattern series. The second column of Fig. 17 illustrates the input signals applied to the input terminals I1, I2 and I3 of the CMOS IC, the third column shows the signals generated on the signal lines L1, L2,..., L12 of the CMOS IC, and the fourth column shows the signals generated on the output terminals O1 and O2 of the CMOS IC. Here, signals "0", "1", "R" and "F" of the second to the fourth

columns of Fig. 17 indicate each of the signals <"0", "0"> (the first element in <> is the start signal value and the second elecment is the final signal value) which is always low, <"1", "1"> which is always high, <"0", "1"> which is a rising signal from low level to high level, and <"1", "0"> which is a falling signal from high level to low level, respectively. Therefore, each test pattern series is composed of two test patterns, for example , the test pattern series T1="00 R" means I1I2I3 =<"000","001">. The fifth column of Fig. 17 shows the set of the defective signal lines detectable by the test using transient power supply current when each test pattern series is applied, i.e. the defect points list. When a signal line has an open defect, the transient power supply current of the IC to be tested becomes abnormal because the switching operation of the logic gate whose input is provided through the defective signal line and thus the transient power supply current waveform of the logic circuit changes. Therefore, by applying the test pattern series and measuring the transient power supply current whether it is abnormal or not, it can be determined whether the logic circuit has a defect or not for the signal line whose switching operation is occurred by the input test pattern series when the logic gate whose input is provided from the above signal switches.

[0091]

For example, if the test pattern series T6 is applied to the CMOS IC shown in Fig. 16, the signal lines L2, L7, L8, L9, L10 and L11 of the CMOS IC to be tested switches and thus the logic gates G2, G3 and G4 and the buffer G6 switches as denoted by signal 0 or 1 of each point in the figure. The signal line L10 switches but the logic gate G5 whose input is the signal line 10 does not switch. Therefore, when there is a defect on any of the signal lines L2, L7, L8, L9 and L11, the abnormality of the transient power supply current is detected by the transient power supply current test having test pattern series T6. Thus, a defect points list for the test pattern series T6 is obtained as LT6= {L2, L7, L8, L9, L11} by the defect simulation as described above.

Method of presuming a defect point (signal line)

Next, a method of presuming a defect point according to the defect

analysis method of the present invention is described in detail. For example, it is considered that the transient power supply current shows abnormality for all the test pattern series when the test pattern series T1, T2 and T6 is applied to the CMOS IC to be tested shown in Fig. 16. According to the result of the defect simulation (Fig. 17), a set of the defective signal lines, i.e. a defect points list (the internal signal lines where a defect may be detected) detectable by each of the test pattern series T2, T4 and T6 is LT1= {L3, L5, L12} , LT2= {L3, L4, L5, L7, L8, L9, L10, L11, L12} and LT4= {L3, L4} , respectively. Therefore, the presumed signal lines to be defective are the common elements of the sets LT1, LT2 and LT4.

$$LT1 \cap LT2 \cap LT4 = \{L3\} \quad (49)$$

Therefore, the defective signal line is presumed to be L3.

[0092]

Moreover, the defective signal line L3 can be presumed by excluding the points (non-defect points) which are not included in the defect points lists LT1 and LT4 from the defect points list LT2= {L3, L4, L5, L7, L8, L9, L10, L11, L12} of the test pattern series T2 which is set to the standard defect points list. First, the standard defect points LT2 is considered as the following.

{L3, L4, L5, L7, L8, L9, L10, L11, L12}

Next, the non-defect points {L1, L2, L4, L6, L7, L8, L9, L10, L11} which are not included in the defect points lists LT1 are excluded from the standard defect points list. Here, the list of the non-defect points is present as the complementary set of the defect points list LT1 (it is denoted by ~LT1). Therefore, the standard defect points list becomes as following by excluding L4, L7, L8, L9, L10 and L11.

{L3, L5, L12}

Then, the non-defect points ~LT4= {L1, L2, L5, L6, L7, L8, L9, L10, L11, L12} which are not included in the defect points lists LT4 are similarly excluded from the standard defect points list. Then, the standard defect points list becomes as following.

{L3}

Therefore, the defect point is presumed to be L3.

[0093]

Next, it is assumed that the transient power supply current shows abnormality when the test pattern series T10 is applied and the transient power supply current is normal when the test pattern series T6 or T12 is applied to the CMOS IC to be tested shown in Fig. 16. Here, T10 is called as abnormal test pattern series, T6 and T12 as normal test pattern series. According to the result of the defect simulation, a set of the defective signal lines, i.e. a defect points list detectable by each of the test pattern series T10, T6 and T12 is LT10= {L1, L6, L8, L9, L11} , LT6= {L2, L7, L8, L9, L11} and LT12= {L1} , respectively. Here, the defect points included in the defect points list LT6 and LT12 are called as the normal points. That is, the defective signal line is any one of the signal lines in the set LT10, and not the ones in the set LT6 or LT12. Therefore, the presumed signal line to be defective is present as the intersection of the set LT10, the complementary set of LT6 (~LT6= {L1, L3, L4, L5, L6, L10, L12}) and the complementary set of LT12 (~LT12= {L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12}) as the following equation.

$$LT10 \cap \sim LT6 \cap \sim LT12 = \{L6\} \qquad (50)$$

Then, the defective signal line is presumed to be L6. The method as described above is equivalent to the method of excluding the non-defect points included in the defect points lists LT6 and LT12 from the defect points list LT10.

[0094]

As described above, the defective point can be presumed in terms of the signal line. However, the present invention is not limited to presume the defect point in terms of the signal line where the logic gate is connected, it is possible to presume the defect point for the signal lines in the logic gate by the defect simulation on the assumption that the defection is present on the signal line in the logic gate.

It is possible to presume the defect point in terms of the signal transmission path. Generation of the defect points list of this case is now described. Switching status of each part on each of the signal transmission paths for each of the test pattern series is examined from the contents of the memory device where the result of the logic simulation is stored, and if all of the part on a signal transmission path for a

test pattern switches, then the test pattern series and the signal transmission paths is registered to the defect list. For example, in the logic simulation in terms of the logic gate, each of the input terminals, internal nodes and output terminals changes for each of the test pattern series as shown in Fig. 15 in the case of the semiconductor IC shown in Fig. 14. Therefore, in case that the signal transmission path is <I1, N1, N3, O1>, I1 is R, N1 is F, N3 is R and O1 is F for the test pattern series T9, from the result of the logic simulation in the memory device, which means all of the parts on the path are switching. In addition, I1 is R, N1 is F, N3 is R, O1 is F for the test pattern series T10 and T11, which means all of the parts on the path are switching. Therefore, test pattern series T9, T10 and T11 for the signal transmission path <I1, N1, N3, O1>are registered to the defect list or the path <I1, N1, N3, O1> is registered for each of the test pattern series T9, T10 and T11. In the logic simulation in terms of the internal signal line, each of the input terminals, internal signal lines and output terminals changes for each of the test pattern series as shown in Fig. 17 in the case of the semiconductor IC shown in Fig. 16. For example, in case that the signal transmission path is <I3, L3, L5, L12, O2>, I3 is R, L3 is R, L5 is R, L12 is F, and O2 is F for the test pattern series T1, from the result of the logic simulation in the memory device, which means all of the parts on the path are switching. In addition, I3 is R, L3 is R, L5 is R, L12 is F, and O2 is F for the test pattern series T2, which means all of the parts on the path are switching. Therefore, test pattern series T1 and T2 for the signal transmission path <I3, L3, L5, L12, O2> are registered to the defect list or the path <I3, L3, L5, L12, O2> is registered for each of the test pattern series T1 and T2. Here, the signal transmission path registered to the defect list is not limited to the path from the input terminal to the output terminal of the circuit, for example, the signal transmission paths which does not reach to the output terminal such as the paths <I1, N1> and <I1, L1, L6> of the semiconductor IC of Fig. 16 may be the object of the test.

[0095]

By doing this, a defect list is generated for all of the signal

transmission paths where a defect may be present. The defect list of the logic simulation in terms of the logic gate for the semiconductor IC shown in Fig. 14 is shown in Fig. 18, and that of the logic simulation in terms of the internal signal line for the semiconductor IC shown in Fig. 16 is shown in Fig. 40.

For presuming a defect point in terms of the signal transmission path, the similar method as for presuming a defect point in terms of the logic gate or the signal line may be used. If the transient power supply current shows abnormality when the test pattern series T9 and T10 are applied to the CMOS IC of Fig. 14, then the defect points list for the test pattern series T9 is <I1, N1, N3, O1>,<I1, N1, N3, O2> and that for the test pattern series T10 is <I1, N1, N3, O1>. It is presumed that the common element <I1, N1, N3, O1> of two defect points lists is the defective signal transmission path.

[0096]

Or, by excluding the points (non-defect point) <I3, O2>,<I3, N2, N3, O1>,<I3, N2, N3, O2>,<I2, N2, N3, O1>,<I1, N1, N3, O2> which are not included in the defect points list of the test pattern series T10 from the defect points list (the standard defect points list) of the test pattern series T9 <I1, N1, N3, O1>,<I1, N1, N3, O2>, the remaining path <I1, N1, N3, O1> is presumed as the defective signal transmission path.

[0097]

Next, it is assumed that the transient power supply current shows abnormality for the test pattern series T9, but it is normal for the test pattern series T10. In this case, by excluding the defect points list <I1, N1, N3, O1> of the normal test pattern series T10 from the defect points list <I1, N1, N3, O1>,<I1, N1, N3, O2> of the abnormal test pattern series T10, the path <I1, N1, N3, O2> is presumed as the defective signal transmission path.

[0098]

Moreover, the defect analysis method of the present invention is not confined to the CMOS IC, it is applicable to other types of semiconductor ICs.

[0099]

[Embodiments]

Fig. 18 shows an example constitution of the defect analysis apparatus according to an embodiment of the present invention. The defect analysis apparatus 100 comprises an test pattern series input unit 101 for inputting a test pattern series having two or more test patterns to the input terminal of the semiconductor IC DUT to be tested, a transient power supply current detector 102 for measuring the transient power supply current generated when said test pattern series is inputted and determining said transient power supply current is abnormal or not, an abnormal pattern series memory unit 103 for saving a plurality of test pattern series that the transient power supply current of said semiconductor IC CUT is abnormal, a normal pattern series memory unit 104 for saving a plurality of test pattern series that the transient power supply current of said semiconductor IC CUT is normal, a defect points list generator 105 for making the test pattern series and the list of the presumed defect points detected for said test pattern series by conducting defect simulation for each of test pattern series stored in said abnormal pattern series memory unit 103 and said normal pattern series memory unit 104, and a defect point presuming unit 106 for presuming the defect points in said semiconductor IC DUT based on said list of the presumed defect points obtained by said using said defect points list generator 105. The test pattern series input unit 101 may be a digital data generator, such as the data time generator HFS 9009 (mainframe) and HFS 9DG2 (data time generator module) manufactured by Sony Techtronics, a pattern generator of the ATE (automatic testing equipment) for IC, such as the logic tester T6671E pattern generator manufactured by Advantest Corporation, or random pattern generator.

Test of the transient power supply current (pulse width)

Fig. 19 shows an example constitution of the transient power supply current detector 102 according to the embodiment of the present invention. This transient power supply current tester 102a comprises a power supply 201 for supplying current to the semiconductor IC DUT to be tested, a transient power supply current waveform measuring unit 202 for measuring the transient power supply current waveform I_{DDT} generated by the test

pattern series outputted by the test pattern series input unit 101, a delay time estimator 203 for measuring the pulse width of the power supply current waveform I_{DDT} measured by the transient power supply current waveform measuring unit 202 and obtaining the signal transmission time of the test path, a defect detector 204 for determining whether there is a defect or not by comparing the delay time obtained by said a delay time estimator 203 to a predetermined value. The power supply 201 may be a static power supply, such as the voltage/current generator R6144 manufactured by Advantest Corporation, a programmable power supply (PPS) of automatic testing equipment (ATE) for IC, such as the logic tester 6671E manufactured by Advantest corporation, or a condenser having large capacitance. However, it is preferable that the current response is quite rapid for the power supply 201, thus the power supply is placed adjacent to the device DUT. The transient power supply current waveform measuring unit 202 may formed as shown in Fig. 20 or 21.

[0100]

That is, Fig. 20 shows an example constitution of the transient power supply current waveform measuring unit 202 according to the present invention. This transient power supply current waveform measuring unit 202a comprises a current sensor 301 for detecting a current waveform flowing between the power supply terminal of the test circuit DUT and the power supply and transforming it to the voltage waveform, and a waveform measuring unit 302 for measuring the voltage waveform transformed by the current sensor 301. The current sensor 301 may be a current sensor of induction type which transforms the transient power supply current waveform to the voltage waveform using the change of the magnetic field surrounding the power supply line connected between the power supply 201 and DUT, or a current sensor of resistance type which transforms, after inserting a resistor element of small resistance in the power supply line, the transient power supply current waveform flowing through the resistor element to the voltage waveform using Ohm's law. However, it is preferable that the current sensor is small for preventing ringing due to the induction coefficient component of the power supply line on the transient power supply current waveform. The waveform measuring unit 302 may be an oscilloscope, such as the digital oscilloscope TDS784A manufactured by Sony Techtronics, or a digitizer of ATE for IC, such

as the logic tester T6671E manufactured by Advantest Corporation.

[0101]

That is, Fig. 21 shows another example constitution of the transient power supply current waveform measuring unit 202 according to the present invention. This transient power supply current waveform measuring unit 202b comprises a switch 401 serially inserted to the power supply line, a condenser 402 for supplying current to the test circuit DUT, which is connected between the connection point of the switch 401 and the test circuit DUT and ground, a waveform measuring unit 403 for measuring the voltage change v(t) of the terminal of the test circuit DUT side, and a waveform differentiator 404 for time-differentiating the voltage waveform v(t) measured by the waveform measuring unit 403. The current flowing from the condenser 402 to the test circuit DUT when the test circuit is a transient state, i.e. the transient power supply current I_{DDT}, is given as following equation if the capacitance of condenser 402 is C, and the voltage of the test circuit DUT side terminal of the condenser 402 is v(t).

[0102]

$$I_{DDT}=-C\frac{dv(t)}{dt} \qquad (51)$$

[0103]

Therefore, the transient power supply current waveform flowing through the test circuit DUT by time-differentiating the voltage waveform v(t) of the condenser 402. Here, the switch 401 is provided to supply all current flowed into the test circuit DUT to the condenser 402 by removing induction coefficient component or the capacitance component of the power supply line. The waveform measuring unit 403 may be an oscilloscope, such as the digital oscilloscope TDS784A manufactured by Sony Techtronics, or a digitizer of the ATE for IC, such as the logic tester T6671E manufactured by Advantest Corporation.

The delay time estimator 203 and the defect detector 204 may be formed as hardware or software.

[0104]

The delay time estimator 203 and the defect detector 204 may be

formed as hardware or software.

Next, the operation of testing semiconductor IC using the transient power supply current tester 102a is described in detail. Fig. 24 illustrates the procedure of the test method of the transient power supply current according to the present invention. The test pattern series input unit 101 inputs a test pattern series activating the test circuit DUT in step 501. In step 502, the transient power supply current waveform measuring unit 202 measures the transient response waveform I_{DD} of the power supply current flowing into the power supply pin of the test circuit DUT from the power supply. Next, the delay time estimator 203 measures the pulse width t_{PW} of the transient power supply current waveform I_{DDT} measured by the transient power supply current waveform measuring unit 202 to obtain the delay time of the test path in step 503. Last, the defect detector 204 compares, in step 504, the pulse width t_{PW} of the transient power supply current waveform I_{DDT} obtained by the delay time estimator 203 to the predetermined value T', determines that a defect is present when the comparison result satisfies the condition of defect detection in step 505, and that there is no defect when the comparison result does not satisfy the condition of defect detection in step 506, and then the process is finished. Here, the power supply 201 supplies a predetermined voltage, for example, 3.3V constantly to the test circuit DUT through the process of semiconductor IC test, i.e. the steps of 501, 502, 503, 504, 505 and 506. The step 501 of inputting a test pattern series and the step 502 of measuring the transient power supply current waveform are performed nearly at the same time. In the step 502 of measuring the transient power supply current waveform, the transient power supply current waveform may be measured by single or multiple measurement(s). For single measurement, the test pattern series is inputted once, while the test pattern is inputted repeatedly for multiple measurements. In case of multiple measurements, it becomes to the initial state upon inputting the test pattern series, that is, the condenser 402 is charged at every time when the condenser 402 is used.

Test of the transient power supply current (instant value)

Fig. 23 shows another example constitution of the transient power supply current tester 102 according to the embodiment of the present

invention. This transient power supply current tester 102b comprises a power supply for supplying power to the semiconductor IC DUT to be tested, an instant transient power supply current measuring unit 602 for measuring the instant value $i_{DDT}(\tau)$ of the transient power supply current generated by the test pattern series outputted by the test pattern series input unit 101 at a predetermined time τ, and a defect detector 603 for comparing the transient power supply current value $i_{DDT}(\tau)$ measured by the instant transient power supply current measuring unit 602 to a predetermined current value I' and determining whether a delay defect is present or not. The power supply 201 may be the one shown in Fig. 21. The instant transient power supply current measuring unit 602 may be formed as shown in Fig. 24 or 25. The defect detector 603 may be formed as hardware or software.

[0105]

Fig. 24 shows an example constitution of the instant transient power supply current measuring unit 602 according to the embodiment of the present invention. This instant transient power supply current measuring unit 602a has a measuring unit 702 for measuring the voltage value transformed by the current sensor 301 instead of the waveform measuring unit 202 in the transient power supply current measuring unit 202 as shown in Fig. 22. The measuring unit 702 may be a digital multimeter, such as the digital multimeter R6581 manufacture by Advantest Corporation an oscilloscope, such as the digital oscilloscope TDS784A manufactured by Sony Techtronics, or a digitizer of the ATE for IC, such as the logic tester T6671E manufactured by Advantest Corporation.

[0106]

Fig. 25 shows another example constitution of the instant transient power supply current measuring unit 602 according to the embodiment of the present invention. This instant transient power supply current measuring unit 602b has a differential measuring unit 803 for measuring the instant differential value of the voltage waveform v(t) of the test circuit DUT side terminal of the condenser 402 instead of the waveform measuring unit 403 and the waveform differential unit 404 in the transient power supply current measuring unit 202b as shown in Fig. 21. The current flowing from the condenser 402 to the test circuit DUT when the test circuit is a transient state, i.e. the transient power supply current

I_{DDT}, is given as following equation which is the same as equation (51).

[0107]

$$I_{DDT}=-C\frac{dv(t)}{dt} \qquad (52)$$

[0108]

Therefore, the instant value $i_{DDT}(\tau)$ of the transient power supply current flowing through the test circuit DUT by measuring the time-differential value of the voltage waveform v(t) of the condenser 402 at the time τ. Here, the instant differential value of voltage waveform v(t) at time τ may be obtained by dividing the difference between two instant values of v(t) at a very short time interval Δt near the time τ by the time interval Δt as shown as following equation (53). It is preferable that Δt is as short as possible to obtain more accurate instant differential value.

[0109]

$$\left.\frac{dv(t)}{dt}\right|_{t=\tau}=\frac{v(\tau+\Delta t)-v(t)}{\Delta t} \qquad (53)$$

[0110]

Here, the switch 401 is provided to supply all current flowed into the test circuit DUT to the condenser 402 by removing induction coefficient component or the capacitance component of the power supply line. The differential measuring unit 803 may be a digital multimeter, such as the digital multimeter R6581 manufacture by Advantest Corporation an oscilloscope, such as the digital oscilloscope TDS784A manufactured by Sony Techtronics, or a digitizer of the ATE for IC, such as the logic tester T6671E manufactured by Advantest Corporation.

[0111]

Next, the operation of testing semiconductor IC using the transient power supply current tester 102b is described in detail. Fig. 28 illustrates the procedure of the test method of the transient power supply current according to the present invention. The test pattern series input unit 101 inputs a test pattern series activating the test circuit DUT in step 901. In step 902, the instant transient power supply current measuring unit 602 measures the instant value $i_{DDT}(\tau)$ of the power supply

current flowing into the power supply pin of the test circuit DUT from the power supply at a predetermined time τ. Here, as explained above, τ may be obtained by the equation $\tau=T'+\tau_0$, where τ_0 is the time of input transition, and T' is the maximum value of permissible delay time. Last, the defect detector 603 compares, in step 903, the instant value $i_{DDT}(\tau)$ of the transient power supply current obtained by the instant transient power supply current measuring unit 602 to the predetermined value, for example, a typical value $I'(=i_{DDT}(\tau_{max}))$ of power supply current at the time τ_{max} of the output transition time of the logic gate G_{final} which switches last for the circuit without defect, determines that "a defect is present" when the comparison result satisfies the condition of defect detection i_{DDT} in step 904, and that "there is no defect" when the comparison result does not satisfy the condition of defect detection i_{DDT} in step 905, and then the process is finished. Here, the power supply 201 supplies a predetermined voltage, for example, 3.3V constantly to the test circuit DUT through the process of the delay defect test, i.e. the steps of 901, 902, 903, 904 and 905. The step 901 of inputting a test pattern series and the step 902 of measuring the instant value of the transient power supply current are performed nearly at the same time. In the step 902 of measuring the instant value of the transient power supply current, the value may be measured by single measurement or by the method of taking the average of the results of multiple measurements to measure it more accurately. For single measurement, the test pattern series is inputted once, while the test pattern is inputted repeatedly for multiple measurements.

Test of the transient power supply current (integral value)

Fig. 27 shows another example constitution of the transient power supply current tester 102 according to the embodiment of the present invention. This transient power supply current tester 102c comprises a power supply 201 for supplying power to the test circuit, an integral transient power supply current measuring unit 1002 for measuring the integral value Q_{DDT} of the transient power supply current generated by the test pattern series outputted by the test pattern series input unit 101 for a predetermined time period, and a defect detector 1003 for comparing the transient power supply current value Q_{DDT} measured by the

integral transient power supply current measuring unit 1002 to a predetermined current value and determining whether a delay defect is present or not. The power supply 201 may be the one shown in Fig. 1. The integral transient power supply current measuring unit 1002 may be composed of a current sensor 301, a waveform measuring unit 302, and a current integrator 1103 as shown in Fig. 28 or composed of a switch 401, a condenser 402, and a measuring unit 1203 as shown in Fig. 29. The defect detector 1003 may be formed as hardware or software.

[0112]

Fig. 28 shows an example constitution of the integral transient power supply current measuring unit 1002 according to the embodiment of the present invention. In this integral transient power supply current measuring unit 1002a, the voltage value transformed by the current sensor 301 is measured by the waveform measuring unit 302 as shown in Fig. 20, and the integral value of the current waveform measured, for this example, by the waveform measuring unit 1102 for the predetermined time period. The current integrator 1103 may be formed as hardware or software.

[0113]

Fig. 29 shows another example constitution of the integral transient power supply current measuring unit 1002 according to the embodiment of the present invention. According to this integral transient power supply current measuring unit 1002b, the current flowing from the condenser 402 to the test circuit DUT when the test circuit is a transient state, i.e. the transient power supply current I_{DDT} is given as following equation, which is the same as shown in Fig. 21.

[0114]

$$I_{DDT}=-C\frac{dv(t)}{dt} \qquad (54)$$

[0115]

Therefore, the integral value Q_{DDT} of the transient power supply current becomes as following equation.

[0116]

$$Q_{DDT}=\int_{-\infty}^{\infty} I_{DDT}dt$$

$$=-C\int_{-\infty}^{\infty}\frac{dv(t)}{dt}dt = -C[v(t)]_{-\infty}^{\infty} = C[v(-\infty)-v(\infty)] \quad (55)$$

[0117]

Here, v (−∞) and v (∞) indicate the initial and final value of the voltage of the condenser 402, respectively. Therefore, the integral value Q_{DDT} of the transient power supply current flowing through the test circuit DUT by measuring the difference between the initial and final value of the voltage of the condenser 402. Here, it is preferable that the initial voltage value v (−∞) of the condenser 402 is measured slightly before the signal transition of the input signal line of the test path, and the final voltage v (∞) of the condenser 402 is measured slightly after the power supply current becomes quiescent power supply current value I_{DDQ} by switching all of the logic gates on the test path. However, it is difficult to determine the time when the power supply current becomes value I_{DDQ}, therefore, it is possible to measure the final voltage v (∞) of the condenser 402 at the time after a sufficient time passed from the input of the test pattern series. The measuring unit 1203 for measuring these voltages v (−∞) and v (∞) may be a digital multimeter, such as the digital multimeter R6581 manufacture by Advantest Corporation an oscilloscope, such as the digital oscilloscope TDS784A manufactured by Sony Techtronics, or a digitizer of the ATE for IC, such as the logic tester T6671E manufactured by Advantest Corporation.

[0118]

Next, the operation of testing semiconductor IC using the transient power supply current tester 102c is described in detail. Fig. 30 illustrates the procedure of the test method of the transient power supply current according to the present invention. The test pattern series input unit 101 inputs a test pattern series activating the test path in step 1301. In step 1302, the integral transient power supply current measuring unit 1002 measures the integral value Q_{DDT} of the power supply current flowing into the power supply pin of the test circuit DUT from the power supply for a predetermined time period T. Here, T is the time period,

for example, from time $\tau(-\infty)$ slightly before the input transition to the time $\tau(\infty)$ until the test circuit is stabilized sufficiently. Last, the defect detector 1003 compares, in step 1303, the integral value Q_{DDT} of the transient power supply current obtained by the integral transient power supply current measuring unit 1002 to the predetermined value $Q_{DDT,\ typ}+\Delta_Q$, and determines that "a defect is present" when the comparison result satisfies the condition of defect detection $Q_{DDT} > Q_{DDT,\ typ}+\Delta_Q$ in step 1304, and that "there is no defect" when the comparison result does not satisfy the condition of defect detection $Q_{DDT} < Q_{DDT,\ typ}+\Delta_Q$ in step 1305, and then the process is finished. Here, the power supply 201 supplies a predetermined voltage, for example, 3.3V constantly to the test circuit DUT through the process of the delay defect test, i.e. the steps of 1301, 1302, 1303, 1304 and 1305. The step 1301 of inputting a test pattern series and the step 1302 of measuring the integral value of the transient power supply current are performed nearly at the same time. In the step 1302 of measuring the integral value of the transient power supply current, the value may be measured by single measurement or by the method of taking the average of the results of multiple measurements to measure it more accurately. For single measurement, the test pattern series is inputted once, while the test pattern is inputted repeatedly for multiple measurements.

Defect analysis

Next, the operation of defect analysis of semiconductor IC using the defect analysis apparatus 100 is described in detail. Fig. 31 illustrates the procedure of defect analysis method. The test pattern series input unit 101 inputs a test pattern series selected from a prepared set of test pattern series to the test circuit DUT in step 1301. The test pattern series inputted to the test circuit DUT is transmitted to the transient power supply current tester 102 almost simultaneously. Next, in step 1402, the transient power supply current tester 102 measures the transient power supply current flowing into the power supply pin of the test circuit DUT from the power supply, and test the circuit DUT. The transient power supply current tester 102 analyzes the result of the transient power supply current test in step 1403, If the transient

power supply current is abnormal, the transient power supply current tester 102 saves the test pattern series used in the test in the abnormal pattern series memory unit 103 in step 1404, and if the transient power supply current is normal, the transient power supply current tester 102 saves the test pattern series used in the test in the normal pattern series memory unit 104 in step 1405. Next, the defect analysis apparatus 100, in step 1406, determines whether there is a test pattern series which is not processed in said set of test pattern series. If there is a test pattern series which is not processed, the steps 1401, 1402, 1403, 1404 and 1405 are repeated, and if there is no test pattern series which is not processed, the method proceeds to step 1407. Next, in step 1407, the defect points list generator 105 conducts a defect simulation for the test pattern series stored in the abnormal pattern series memory unit 103 and the normal pattern series memory unit 104 and generates a list of the points where defects are detectable (defect points list). That is, logical simulation determining where the logical value of the signal changes when the test pattern series is inputted to the test circuit without defect is performed, and the points where defects are detectable is obtained by the point where the logical value changes. In step 1408, the defect point presuming unit 106 presumes defect point(s) based on the defect points list generated by the defect points list generator 105 according to the method explained with reference to Figs. 14 to 19. Then, it is determined whether the result of presuming defect points is sufficient or not in step 1409. If the test circuit is very complicated, it is difficult to confine the defect points to a single point. In this case, number of the presumed defect points is, for example, 10, it can be determined that the result is sufficient because the presumed defect points can be examined using electron beam tester in relatively short time period. That is, in step 1409, it is determined that the number of the presumed defect points are decreased to the predetermined number or not. If the result of the presuming defect points is not sufficient, the process proceeds to step 1410, and if the result of the presuming defect points is sufficient, the process is finished. When the result of the presuming defect points is not sufficient, the defect analysis apparatus 100 determines whether there is a test pattern series which is not processed in the abnormal pattern series memory unit 103 and the

normal pattern series memory unit 104 in step 1410. If there is a test pattern series which is not processed, the steps 1407 and 1408 are repeated, and if there is no test pattern series which is not processed, the process is finished. Here, any one of the methods shown in Figs. 22, 26 and 30 may be used for the test of the transient power supply current of step 1402.

[0119]

Fig. 32 illustrates another procedure of defect analysis method of the present invention. The test pattern series input unit 101 inputs a test pattern series selected from a prepared set of test pattern series to the test circuit DUT in step 1501. The test pattern series inputted to the test circuit DUT is transmitted to the transient power supply current tester 102 almost simultaneously. Next, in step 1502, the transient power supply current tester 102 measures the transient power supply current flowing into the power supply pin of the test circuit DUT from the power supply, and test the circuit DUT. The transient power supply current tester 102 analyzes the result of the transient power supply current test in step 1503, If the transient power supply current is abnormal, the transient power supply current tester 102 saves the test pattern series used in the test in the abnormal pattern series memory unit 103 in step 1504, and if the transient power supply current is normal, the transient power supply current tester 102 saves the test pattern series used in the test in the normal pattern series memory unit 104 in step 1505. Next, in step 1506, the defect points list generator 105 generates a defect points list for the test pattern series stored in the abnormal pattern series memory unit 103 and the normal pattern series memory unit 104 obtained by the transient power supply current test. In step 1507, the defect point presuming unit 106 presumes defect point(s) based on the defect points list generated by the defect points list generator 105. Then, it is determined whether the result of presuming defect points is sufficient or not in step 1508. If the result of the presuming defect points is not sufficient, the process proceeds to step 1509, and if the result of the presuming defect points is sufficient, the process is finished. When the result of the presuming defect points is not sufficient, the defect analysis apparatus 100 determines whether there is a test pattern series which is not processed in the set of test

pattern series in step 1509. If there is a test pattern series which is not processed, the steps 1501, 1502, 1503, 1504, 1505, 1506, 1507 and 1508 are repeated, and if there is no test pattern series which is not processed, the process is finished. Here, any one of the methods shown in Figs. 22, 26 and 30 may be used for the test of the transient power supply current of step 1502. For presuming a defect point in step 1507 according to the method shown in Fig. 32, the method of excluding, from the standard defect points list based on the first detected abnormality, the elements which is not included in the defect points lists based on abnormality detected later.

Presuming a defect point

Fig. 33 shows an example constitution of the defect point presuming unit 106 according to the embodiment of the present invention. This defect point presuming unit 106a comprises a defect points list memory unit 1601 for storing a plurality of defect points lists generated by the defect points list generator 105 for a plurality of abnormal test pattern series, where the transient power supply current is abnormal, stored in the abnormal pattern series memory unit 103 and a common defect point presuming unit 1602 for presuming a defect point which is included in the plurality of defect points lists stored in the defect points list memory unit 1601 in common. The defect points list memory unit 1601 may be a physical recording medium like a hard disk or a memory, or a virtual memory established on the memory. The common defect point presuming unit 1602 may be formed as hardware or software. In the example of Fig. 33, the normal pattern series memory unit 104 may be omitted.

[0120]

Next, the operation of presuming a defect point using the defect point presuming unit 106a is described in detail. Fig. 36 illustrates the procedure of defect point presuming method of the present invention. First, the defect points list generator 105 gets an abnormal test pattern series stored in the abnormal pattern series memory unit 103 in step 1701. Next, in step 1702, the defect points list generator 105 generates a defect points list by performing a defect simulation for the abnormal test pattern series obtained in step 1701. In step 1703, the defect points list generated by the defect points list generator 105 is transmitted

to and stored in the defect points list memory unit 1601. Next, it is determined whether there is an abnormal test pattern series which is not processed or not for the abnormal pattern series memory unit 103. If there is an abnormal test pattern series which is not processed, the steps 1701, 1702 and 1703 are repeated, and if there is no abnormal test pattern series which is not processed, the method proceeds to step 1705. Last, in step 1705, the common defect points presuming unit 1602 presumes the defect points which are included in all of the defect points lists stored in the defect points list memory unit 1601 in common, and the process is finished. For the presuming defect points, step 1407 and 1408 of Fig. 31 or step 1506 and 1507 of Fig. 32 may be used.

[0121]

Fig. 35 shows another example constitution of the defect point presuming unit 106 according to the embodiment of the present invention. This defect point presuming unit 106b comprises a standard defect points list memory unit 1801 for storing a defect points lists generated by the defect points list generator 105 for the abnormal test pattern series, where the abnormality of the transient power supply current is detected first, stored in the abnormal pattern series memory unit 103 and a non-defect point excluding unit 1802 for storing defect points lists generated by the defect points list generator 105 for the rest of the abnormal test pattern series stored in the abnormal pattern series memory unit 103 except the test pattern series used to generate the standard defect points list and excluding, from the standard defect points list stored in the standard defect points list memory unit 1801, the defect points except the points which are included in said defect points lists (non-defect points). The standard defect points list memory unit 1801 may be a physical recording medium like a hard disk or a memory, or a virtual memory established on the memory. The non-defect point excluding unit 1802 may be formed as hardware or software. In the example of Fig. 35, the normal pattern series memory unit 104 may be omitted.

[0122]

Next, the operation of presuming a defect point using the defect point presuming unit 106b is described in detail. Fig. 36 illustrates the procedure of defect point presuming method of the present invention. First, the defect points list generator 105 gets an abnormal test pattern

series, where the transient power supply current shows abnormality first, stored in the abnormal pattern series memory unit 103 in step 1901. Next, in step 1902, the defect points list generator 105 generates a standard defect points list by performing a defect simulation for the abnormal test pattern series obtained in step 1901. In step 1903, the standard defect points list generated by the defect points list generator 105 is transmitted to and stored in the standard defect points list memory unit 1801. Then, in step 1904, the defect points list generator 105 gets another abnormal test pattern series from the rest of the abnormal test pattern series in the abnormal test pattern series memory unit 103. Next, in step 1905, the defect points list generator 105 generates another standard defect points list by performing a defect simulation for the abnormal test pattern series obtained in step 1904. In step 1906, the non-defect point excluding unit 1802 excludes, from the standard defect points list, the defect points except the points which are included in said defect points lists generated in step 1905 (non-defect points) based on the defect points lists generated by the defect points lists generator 105. Last, it is determined whether there is an abnormal test pattern series which is not processed or not for the abnormal pattern series memory unit 103. If there is an abnormal test pattern series which is not processed, the steps 1904, 1905 and 1906 are repeated, and if there is no abnormal test pattern series which is not processed, the process is finished. For the presuming defect points, step 1407 and 1408 of Fig. 31 or step 1506 and 1507 of Fig. 32 may be used. However, if there is no abnormal test pattern series to get in step 1904, the method for presuming defect point is finished immediately.

[0123]

Fig. 37 shows another example constitution of the defect point presuming unit 106 according to the embodiment of the present invention. This defect point presuming unit 106c comprises an abnormal defect points list memory unit 2001 for storing a plurality of defect points lists generated by the defect points lists generator 105 for a plurality of test pattern series, where the transient power supply current is abnormal, stored in the abnormal pattern series memory unit 103, a normal defect points list memory unit 2002 for storing a plurality of defect points lists generated by the defect points lists generator 105 for a plurality

of test pattern series, where the transient power supply current is normal, stored in the normal pattern series memory unit 104, a common defect point presuming unit 2003 for presuming the possible defect points by extracting the defect points which are included in all of the defect points list stored in said abnormal defect points list memory device 2001 in common, a possible defect points list memory unit 2004 for storing the possible defect points list generated by the common defect point presuming unit 2003, and a non-defect points excluding unit 2005 for excluding the defect point which is included in the plurality of defect points lists stored in the normal defect points list memory unit 2002 from the possible defect points list one by one. The abnormal defect points list memory unit 2001, normal defect points list memory unit 2002 and the possible defect points list memory unit 2004 may be formed of physical recording media like hard disks or memories, or virtual memories established on the memory. The common defect point presuming unit 2003 and the non-defect points excluding unit 2005 may be formed as hardware or software.

[0124]

Next, the operation of presuming a defect point using the defect point presuming unit 106c is described in detail. Fig. 38 illustrates the procedure of defect point presuming method of the present invention. First, the defect points list generator 105 gets an abnormal test pattern series stored in the abnormal pattern series memory unit 103 in step 1901. Next, in step 2102, the defect points list generator 105 generates a defect points list by performing a defect simulation for the abnormal test pattern series obtained in step 2101. In step 2103, the defect points list generated by the defect points list generator 105 is transmitted to and stored in the abnormal defect points list memory unit 2001. Then, in step 2104, it is determined whether there is an abnormal test pattern series which is not processed for the abnormal pattern series memory unit 103. If there is an abnormal test pattern series which is not processed, the steps 2101, 2102 and 2103 are repeated, and if there is no abnormal test pattern series which is not processed, the process is proceed to step 2105. Next, in step 2105, the common defect point presuming unit 2003 presumes the possible defect points by extracting the defect points which are included in all of the defect points list stored in said abnormal

defect points list memory device 2001 in common and generates a possible defect points list. Then, the common defect point presuming unit 2003 transmits and stores possible defect points list to the possible defect points list memory unit 2004. Next, in step 2107, the defect points list generator 105 gets a normal test pattern series from the normal test pattern series memory unit 104. Then, the defect points list generator 105 generates a defect points list by performing a defect simulation for the normal test pattern series obtained in step 2107. In step 2109, the non-defect points excluding unit 2005 excludes the defect point which is included in the defect points lists generated by the defect points list generator 105 in step 2108 (non-defect point) from the possible defect points list. Last, in step 2110, it is determined whether there is an normal test pattern series which is not processed. If there is a normal test pattern series which is not processed, the steps 2107, 2108 and 2109 are repeated, and if there is no normal test pattern series which is not processed, the process is finished. For the presuming defect points, step 1407 and 1408 of Fig. 31 or step 1506 and 1507 of Fig. 32 may be used. However, if there is no abnormal test pattern series in step 2101, or if there is no normal test pattern series in step 2107, the method for presuming defect point is finished immediately.

[0125]

In the above description, a defect points list is obtained upon request by a defect simulation, however, it is possible to obtain a defect points list by referring the reference table storing the test pattern series and corresponding defect points list while the defect simulations are conducted for various test pattern series in advance.

According to the method and apparatus for defect analysis of the present invention, a defect point may be presumed in terms of logic gate by appointing a defect point in terms of logic gate for the defect simulation. Moreover, a defect point may be presumed in terms of signal line by appointing a defect point in terms of signal line for the defect simulation. In addition, the method and apparatus for defect analysis of the present invention presume the defect such as a logical defect (stuck defect), short defect or defect of parameter delinquency of MOS transistors as well as the delay defect or disconnection defect.

[0126]

[Effect of the Invention]

As described above, the reliability of the defect analysis is improved largely because a delay defect or a disconnection defect accompanying a delay defect can be presumed using a method of testing the transient power supply current which is easily observed and having switching information of logic gates.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1] 1A shows an example response of the output voltage V_{OUT} for the change of input voltage V_{IN} of CMOS inverter over time and an example transient response of the current I_{DD} for the change of input voltage V_{IN} over time, 1B illustrates the CMOS inverter circuit and the power supply current flowing at rising transition of output, and 1C shows the CMOS inverter circuit and the power supply current flowing at falling transition of output.

[Fig. 2] 2A shows the transmission characteristics of input voltage V_{IN}, output voltage V_{OUT} and power supply current for the typical example of the transient response of the CMOS logic gate, and 2B shows the approximate waveform of the transient current.

[Fig. 3] 3A is a circuit diagram of an example CMOS IC, and 3B shows the changes of input voltage and output voltages for the IC and the transient power supply current I_{DDT} corresponding to the change.

[Fig. 4] 4A is a schematic diagram showing the principle of the delay defect test method for the semiconductor having output threshold, and 4B shows the relation between the operation clock CLK and the delay of the output voltage V_{OUT} for the input voltage V_{IN} of the circuit.

[Fig. 5] 5A illustrates a disconnection of a signal line which make a logical defect and the input and output voltages for the signal line, and 5B illustrates a disconnection of a signal line which make a delay defect and the input and output voltages for the signal line.

[Fig. 6] 6A shows the time delay of the input and output voltages in cases that the delay defect is present and not present for CMOS logic circuit, and 6B is a diagram to show the principle of the transient power supply current test method and it illustrates a transient power supply current corresponding to the change of input and output voltages of Fig. 6a.

[Fig. 7] Fig. 7 is a diagram to show the principle of another transient power supply current test method, and A shows the time delay of the input and output voltages in cases that the delay defect is present and not present and B shows corresponding transient power supply current and measuring time.

[Fig. 8] Fig. 8 shows the change of the integral of the transient power supply current for the input transition time of the CMOS inverter.

[Fig. 9] 9A is a model of a minute open defect present in the input signal line of the CMOS inverter, 9B is a schematic diagram showing signal transition time in case that no minute open defect is present, and 9C is a schematic diagram showing signal transition time after the minute open defect in case that tha minute open defect is present.

[Fig. 10] Fig. 10 shows the change of the integral Q_{DDT} of the transient power supply current for the resistance R_{open} for the minute open defect

present in the CMOS IC.

[Fig. 11] Fig. 11 is a bar graph showing the distribution of the transient power supply current of the CMOS IC for the difference of the CMOS fabrication process.

[Fig. 12] Fig. 12 illustrates the change of path delay time t_{pd} of test path for the resistance R_{open} of the minute open defect present on the test path of the CMOS IC.

[Fig. 13] Fig. 13 shows the linearity between the path delay time t_{pd} and the integral Q_{DDT} of the transient power supply current of the CMOS IC.

[Fig. 14] Fig. 14 is a circuit diagram of an example CMOS IC to be tested.

[Fig. 15] Fig. 15 shows an example result of a defect simulation for the test CMOS IC shown in Fig. 14.

[Fig. 16] Fig. 16 is a circuit diagram of another example CMOS IC to be tested.

[Fig. 17] Fig. 17 shows an example result of another defect simulation for the test CMOS IC shown in Fig. 16.

[Fig. 18] Fig. 18 is a block diagram showing an example constitution of the defect analysis apparatus of the present invention.

[Fig. 19] Fig. 19 is a block diagram showing an example constitution of the transient power supply current tester 102 of Fig. 18.

[Fig. 20] Fig. 20 is a block diagram showing an example constitution of the transient power supply current waveform measuring unit 202 of Fig. 19.

[Fig. 21] Fig. 21 is a block diagram showing another example constitution of the transient power supply current waveform measuring unit 202 of Fig. 19.

[Fig. 22] Fig. 22 is a flowchart illustrating an example process sequence of the transient power supply current test method which can be used as the defect analysis method of the present invention.

[Fig. 23] Fig. 23 is a block diagram showing another example constitution of the transient power supply current tester 102 of Fig. 18.

[Fig. 24] Fig. 24 is a block diagram showing an example constitution of the instant transient power supply current measuring unit 602 of Fig. 23.

[Fig. 25] Fig. 25 is a block diagram showing another example constitution of the instant transient power supply current measuring unit 602 of Fig. 23.

[Fig. 26] Fig. 26 is a flowchart illustrating another example process sequence of the transient power supply current test method which can

be used as the defect analysis method of the present invention.

[Fig. 27] Fig. 27 is a block diagram showing more another example constitution of the transient power supply current tester 102 of Fig. 18.

[Fig. 28] Fig. 28 is a block diagram showing an example constitution of the integral transient power supply current measuring unit 1002 of Fig. 27.

[Fig. 29] Fig. 29 is a block diagram showing an example constitution of the integral transient power supply current measuring unit 1002 of Fig. 27.

[Fig. 30] Fig. 30 is a flowchart illustrating more another example process sequence of the transient power supply current test method which can be used as the defect analysis method of the present invention.

[Fig. 31] Fig. 31 is a flowchart illustrating an example process sequence of the defect analysis method of the present invention.

[Fig. 32] Fig. 32 is a flowchart illustrating another example process sequence of the defect analysis method of the present invention.

[Fig. 33] Fig. 33 is a block diagram showing an example constitution of the defect point presuming unit 106 of Fig. 18.

[Fig. 34] Fig. 34 is a flowchart illustrating an example process sequence of method for presuming defect point which can be used as the

defect analysis method of the present invention.

[Fig. 35] Fig. 35 is a block diagram showing another example constitution of the defect point presuming unit 106 of Fig. 18.

[Fig. 36] Fig. 36 is a flowchart illustrating another example process sequence of method for presuming defect point which can be used as the defect analysis method of the present invention.

[Fig. 37] Fig. 37 is a block diagram showing more another example constitution of the defect point presuming unit 106 of Fig. 18.

[Fig. 38] Fig. 38 is a flowchart illustrating more another example process sequence of method for presuming defect point which can be used as the defect analysis method of the present invention.

[Fig. 39] Fig. 39 shows an example defect points list in terms of signal transmission path for the circuit shown in Fig. 14.

[Fig. 40] Fig. 40 shows an example defect points list in terms of signal transmission path for the circuit shown in Fig. 16.

JAPANESE PATENT APPLICATION NO.2000-101867

[DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECT] To efficiently presume an internal defect point of a delay defect and/or open defect, without fabricating a semiconductor IC device.

[MEANS FOR ACHIEVING THE OBJECT] Inputting a test pattern series comprising two or more test patterns to an input/output terminal of a semiconductor IC under test; measuring a transient power supply current generated of said semiconductor IC under test generated when said test pattern series is input and determining whether said transient current shows abnormality or not; obtaining a list (defect point list) of points at which a defect can be detected for said test pattern series indicating an abnormality in the transient power supply current; and presuming a defect point inside said semiconductor IC circuit under test based on said defect point list.

[SELECTED FIGURE] Fig. 31

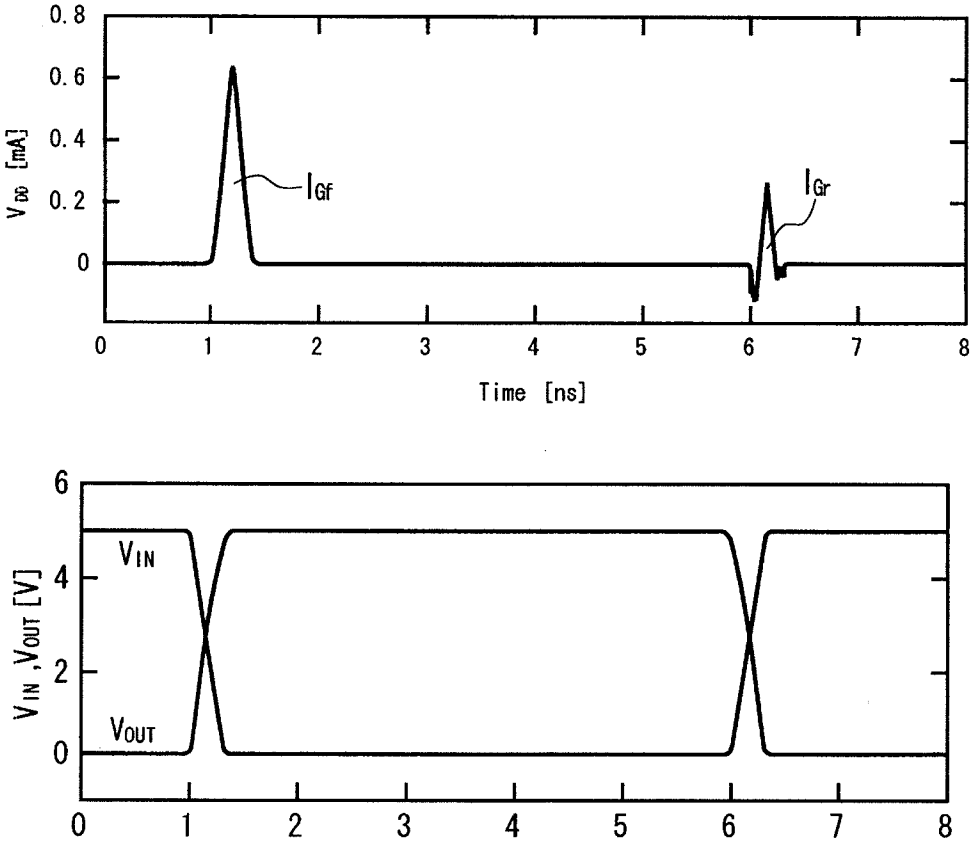


FIG. 1A

FIG. 1B

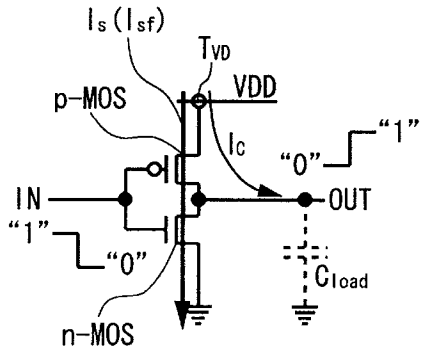


FIG. 1C

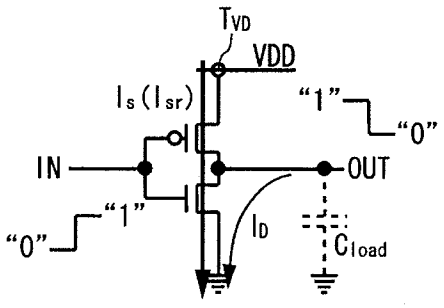


FIG. 2A

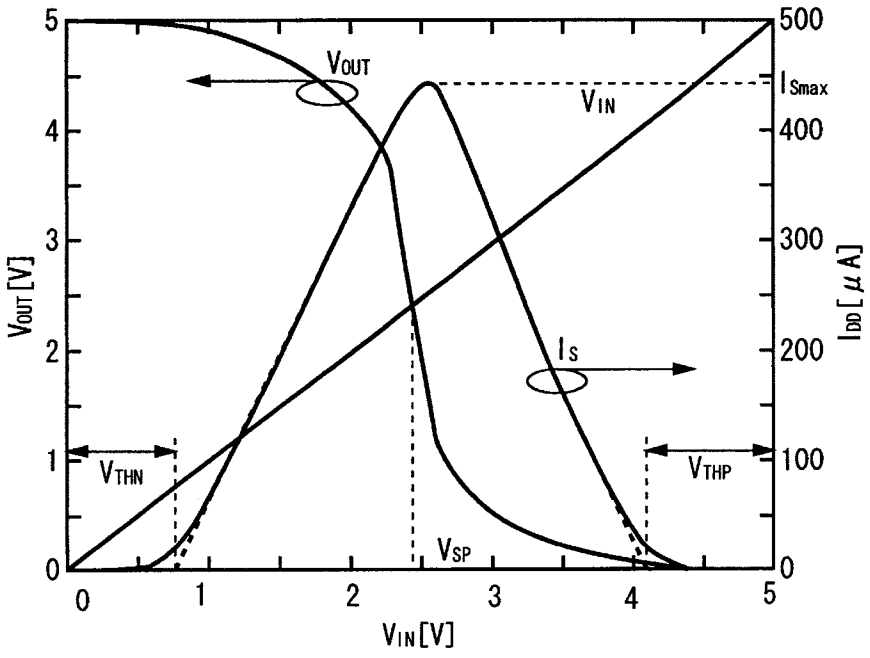

VOUT
VIN
ISmax
IS
VTHN
VTHP
VSP
VOUT[V]
IDD[μA]
VIN[V]
0
1
2
3
4
5
100
200
300
400
500

FIG. 2B

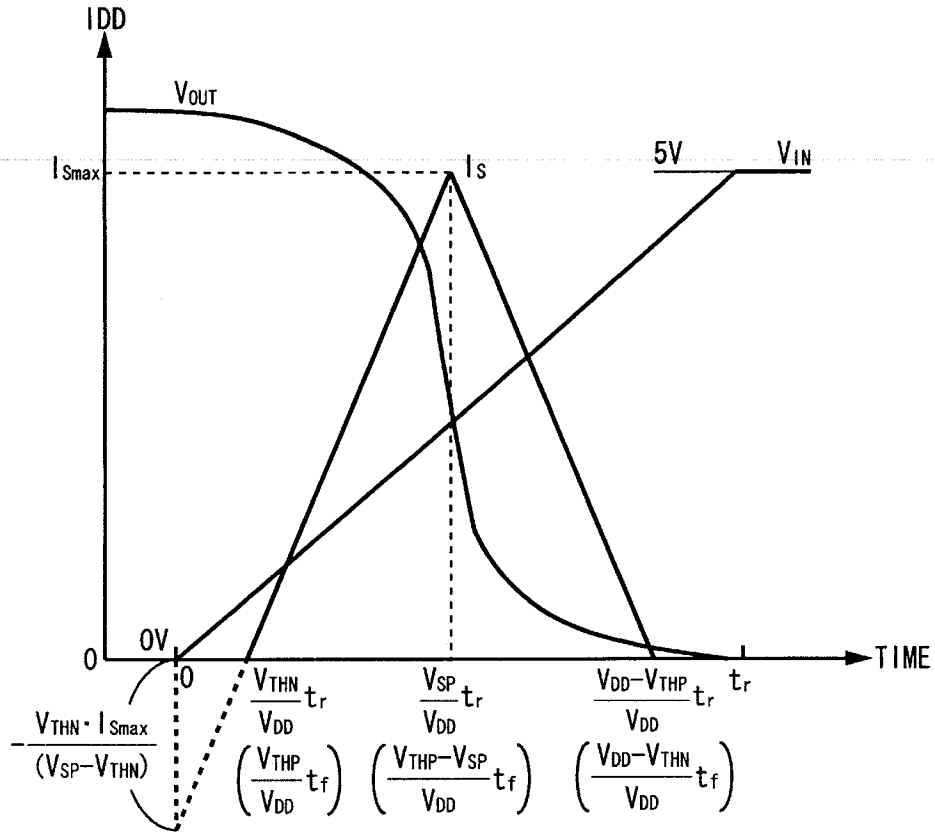

IDD
VOUT
ISmax
IS
5V
VIN
0V
0
TIME
VTHN·ISmax / (VSP−VTHN)
VTHN/VDD tr
VSP/VDD tr
VDD−VTHP/VDD tr
tr
(VTHP/VDD tf)
(VTHP−VSP/VDD tf)
(VDD−VTHN/VDD tf)

FIG. 3A

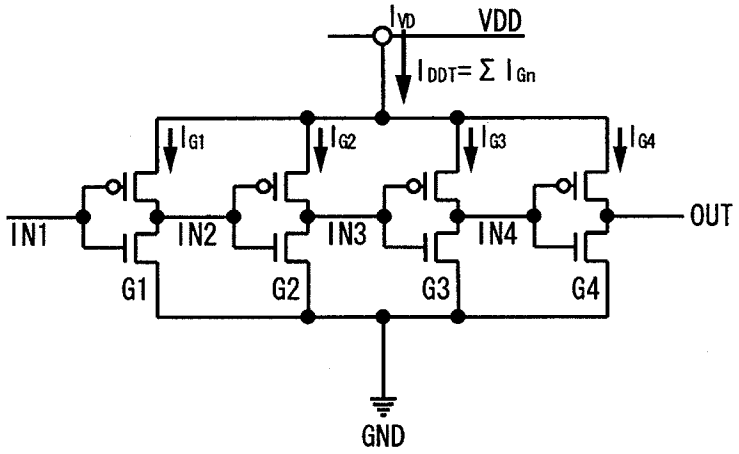
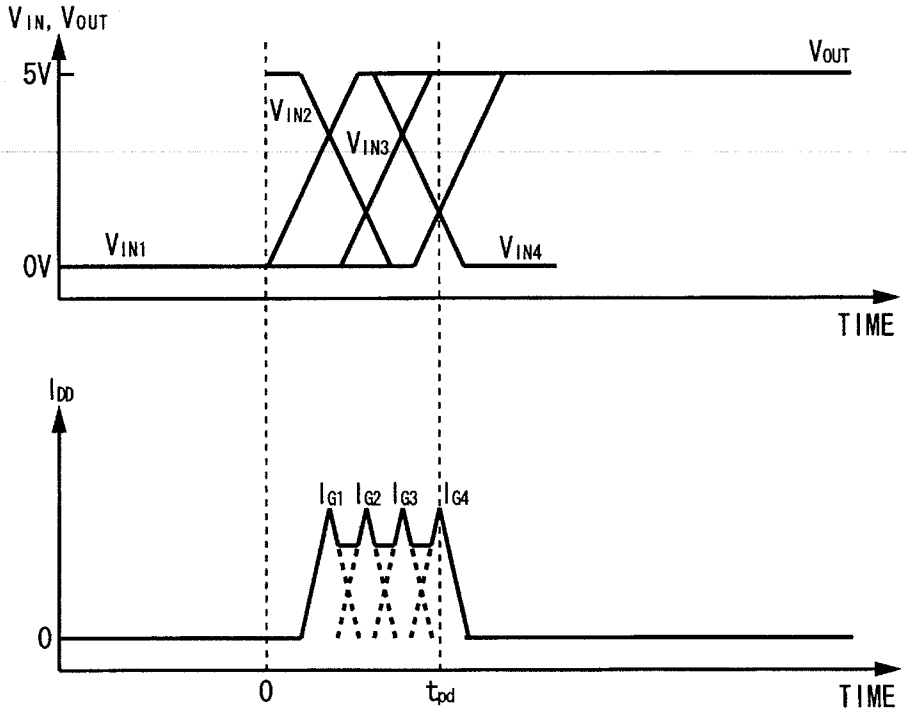

IVD
VDD
IDDT= Σ IGn
IG1
IG2
IG3
IG4
IN1
IN2
IN3
IN4
OUT
G1
G2
G3
G4
GND

FIG. 3B


VIN, VOUT
5V
0V
VIN1
VIN2
VIN3
VIN4
VOUT
TIME
IDD
IG1 IG2 IG3 IG4
0
0
tpd
TIME

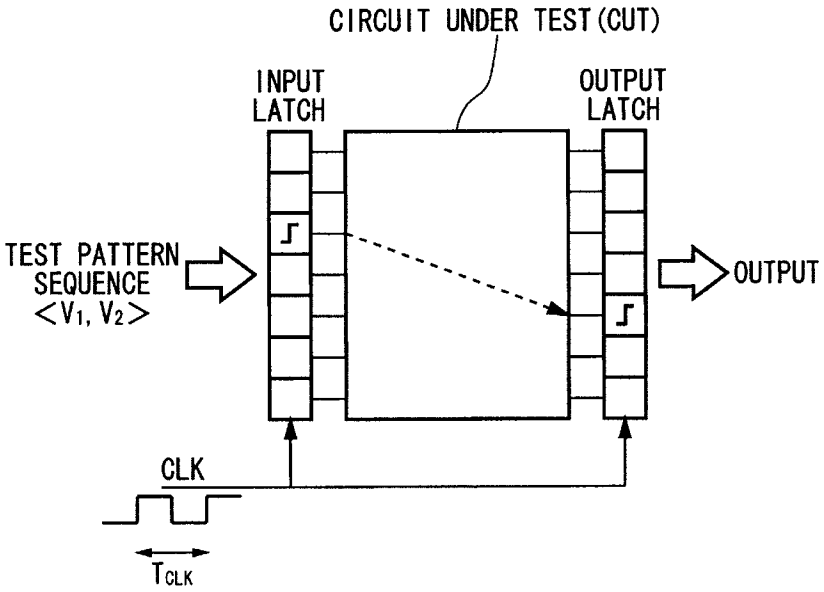

CIRCUIT UNDER TEST (CUT)
INPUT LATCH
OUTPUT LATCH
TEST PATTERN SEQUENCE
<V1, V2>
OUTPUT
CLK
TCLK

FIG. 4A

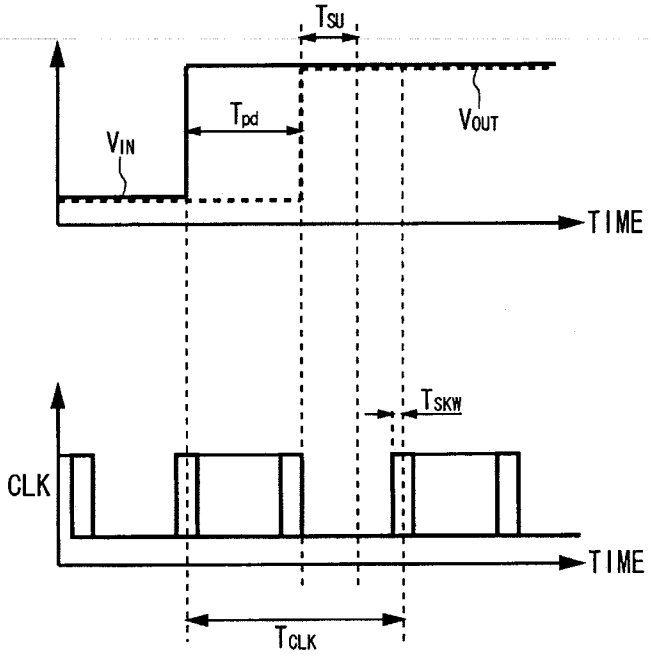

TSU
Tpd
VIN
VOUT
TIME
TSKW
CLK
TIME
TCLK

FIG. 4B

FIG. 5A

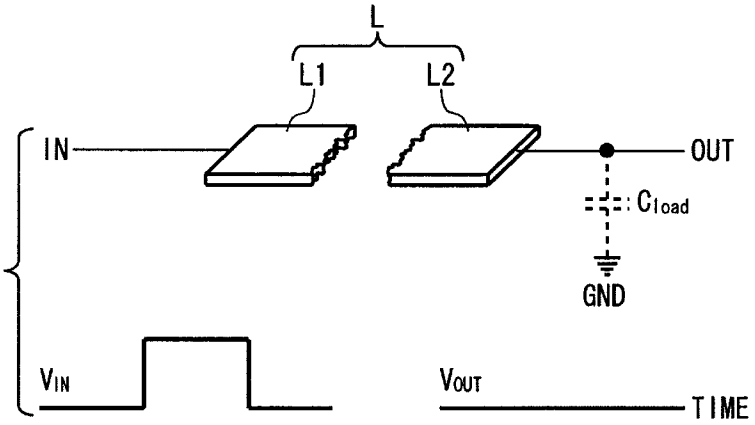

L
L1
L2
IN
OUT
Cload
GND
VIN
VOUT
TIME

FIG. 5B

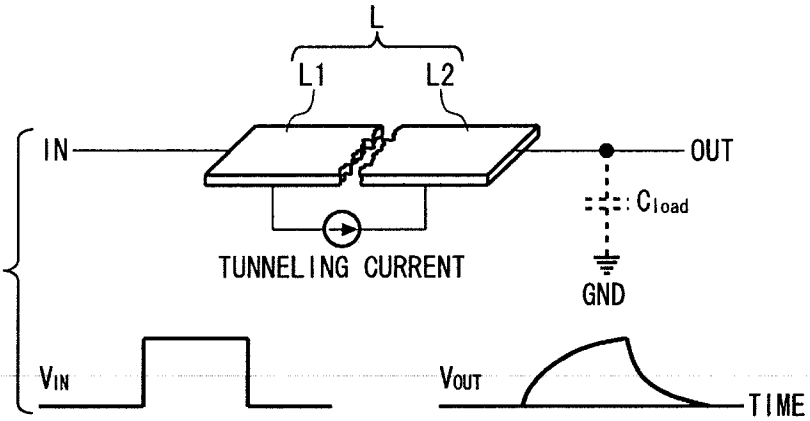

L
L1
L2
IN
OUT
Cload
TUNNELING CURRENT
GND
VIN
VOUT
TIME

FIG. 6A

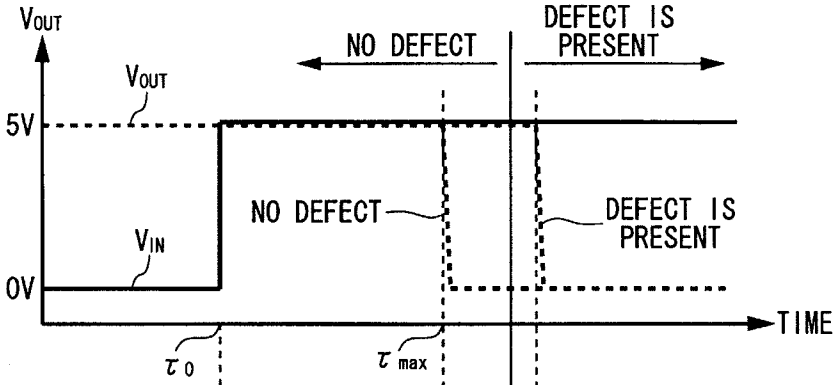

VOUT
NO DEFECT
DEFECT IS PRESENT
VOUT
5V
VIN
0V
NO DEFECT
DEFECT IS PRESENT
TIME
τ 0
τ max

FIG. 6B

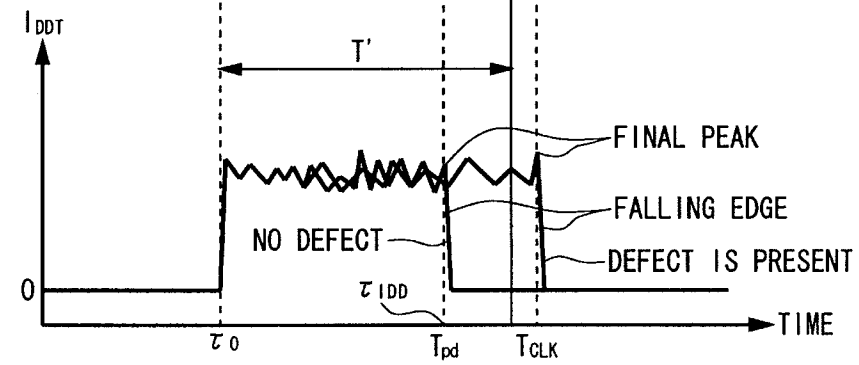

IDDT
T'
FINAL PEAK
FALLING EDGE
NO DEFECT
DEFECT IS PRESENT
0
τ IDD
TIME
τ 0
Tpd
TCLK

FIG. 7A

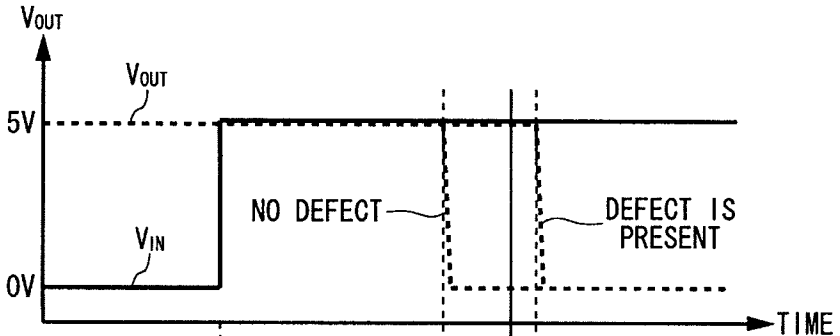
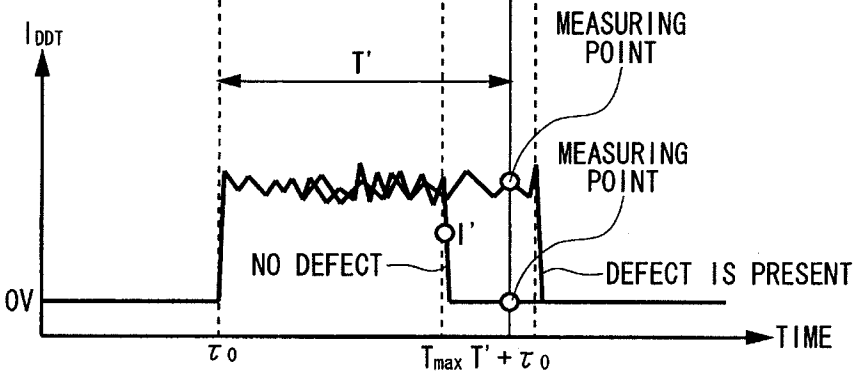


FIG. 7B



NO DEFECT: $i_{DDT}(T'+\tau_0) \leqq I'$

DEFECT IS PRESENT: $i_{DDT}(T'+\tau_0) > I'$

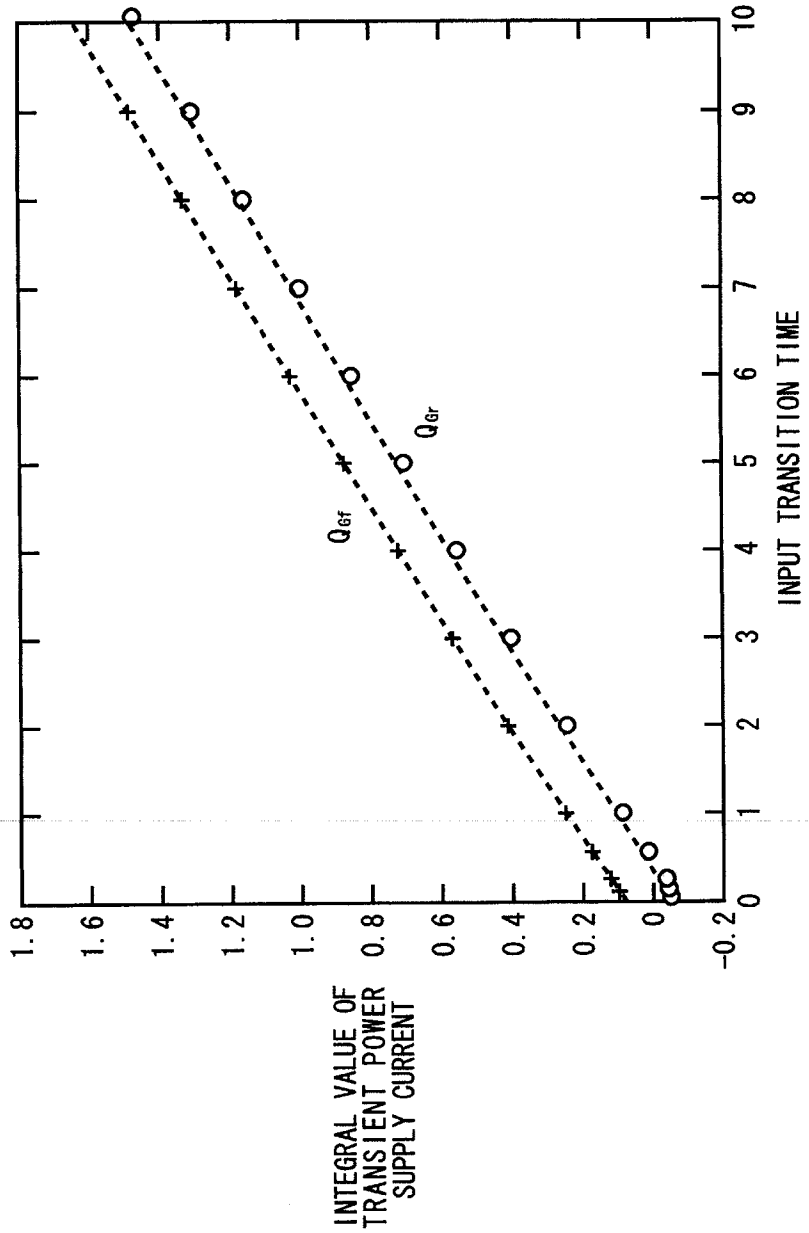

INTEGRAL VALUE OF TRANSIENT POWER SUPPLY CURRENT
INPUT TRANSITION TIME
Q_{Gf}
Q_{Gr}
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
−0.2
0
1
2
3
4
5
6
7
8
9
10

FIG. 8

FIG. 9A

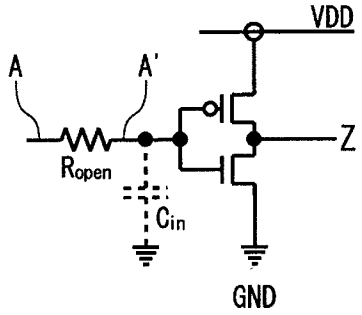


FIG. 9B

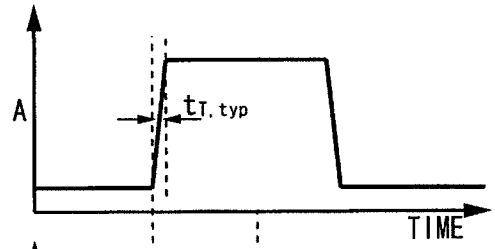
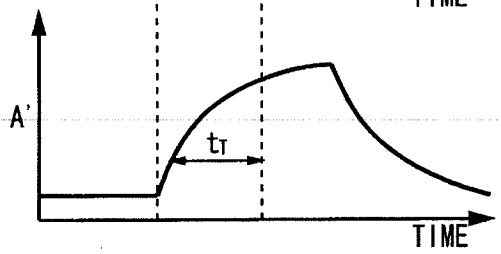


FIG. 9C



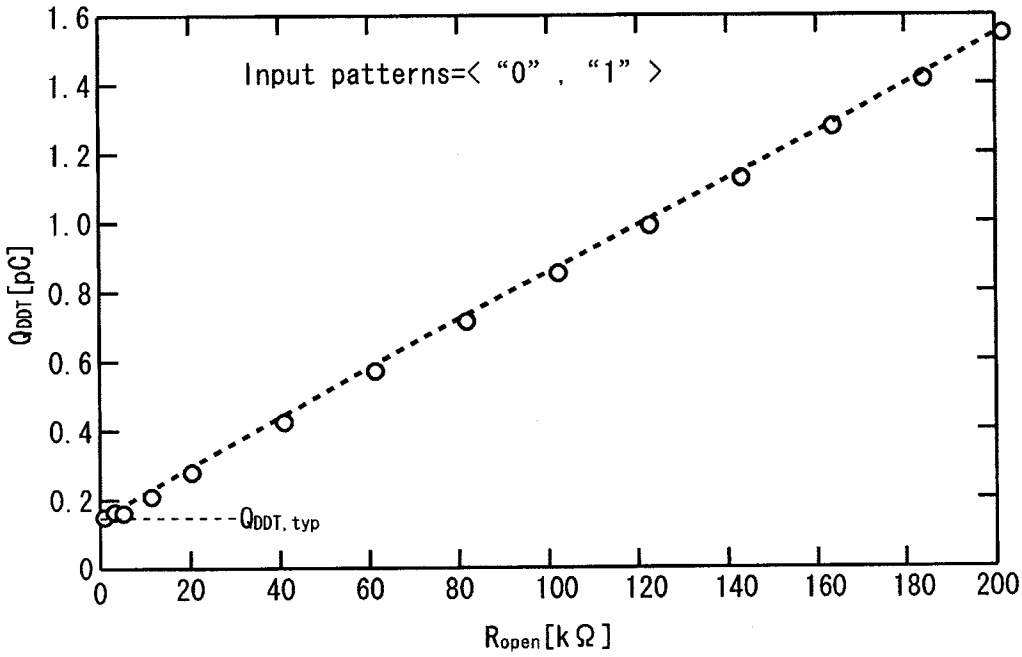

Input patterns=< "0" , "1" >
Q_{DDT}[pC]
R_{open}[kΩ]
$Q_{DDT,typ}$
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
140
160
180
200

FIG. 10

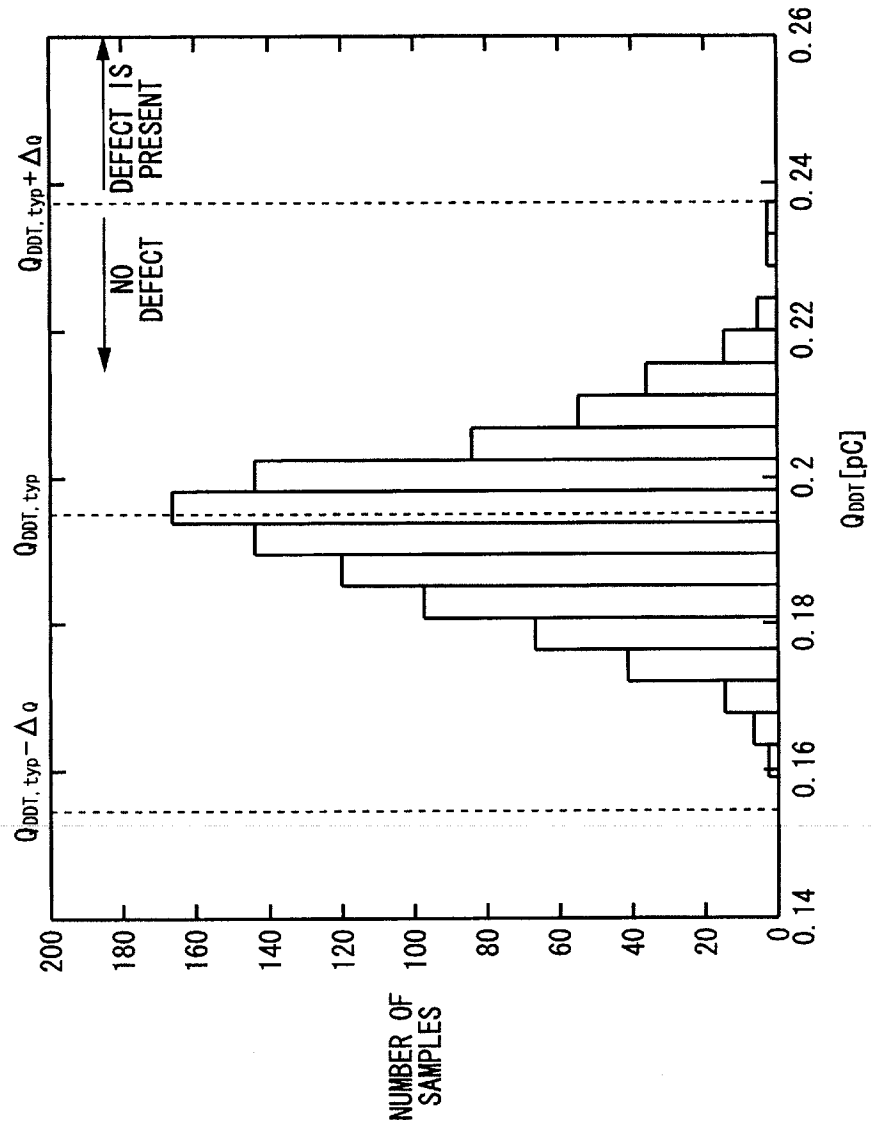

DEFECT IS PRESENT
NO DEFECT
$Q_{DDT, typ}+\Delta_Q$
$Q_{DDT, typ}$
$Q_{DDT, typ}-\Delta_Q$
NUMBER OF SAMPLES
Q_{DDT} [pC]
0
20
40
60
80
100
120
140
160
180
200
0.14
0.16
0.18
0.2
0.22
0.24
0.26

FIG. 11

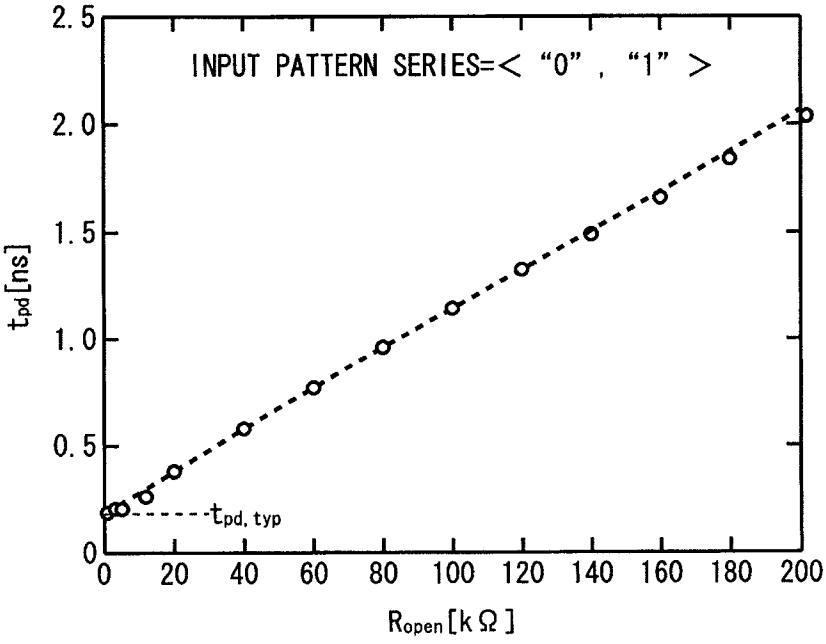

INPUT PATTERN SERIES=< "0" , "1" >
t_{pd}[ns]
$t_{pd, typ}$
R_{open}[kΩ]
2.5
2.0
1.5
1.0
0.5
0
0
20
40
60
80
100
120
140
160
180
200

FIG. 12

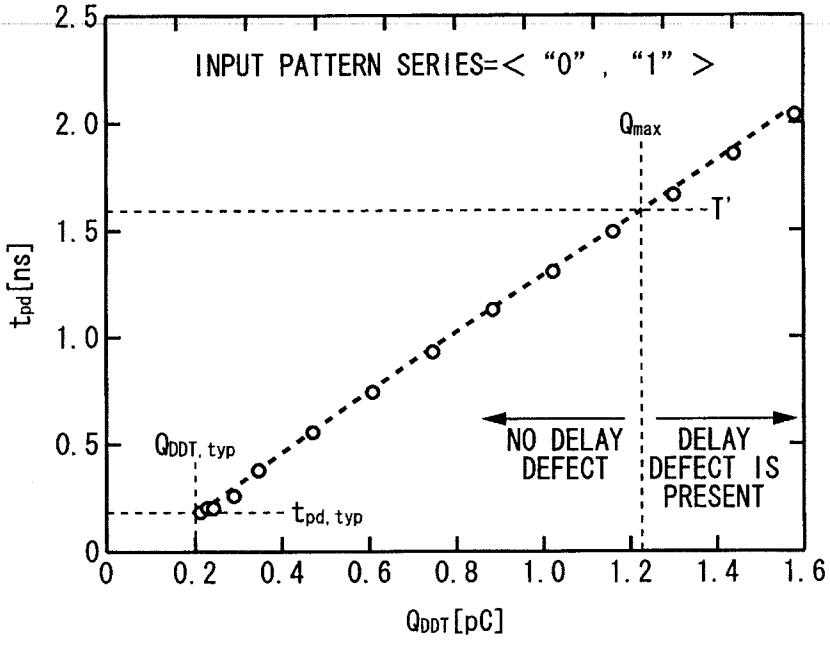

INPUT PATTERN SERIES=< "0" , "1" >
Q_{max}
T'
t_{pd}[ns]
$Q_{DDT, typ}$
$t_{pd, typ}$
NO DELAY DEFECT
DELAY DEFECT IS PRESENT
Q_{DDT}[pC]
2.5
2.0
1.5
1.0
0.5
0
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6

FIG. 13

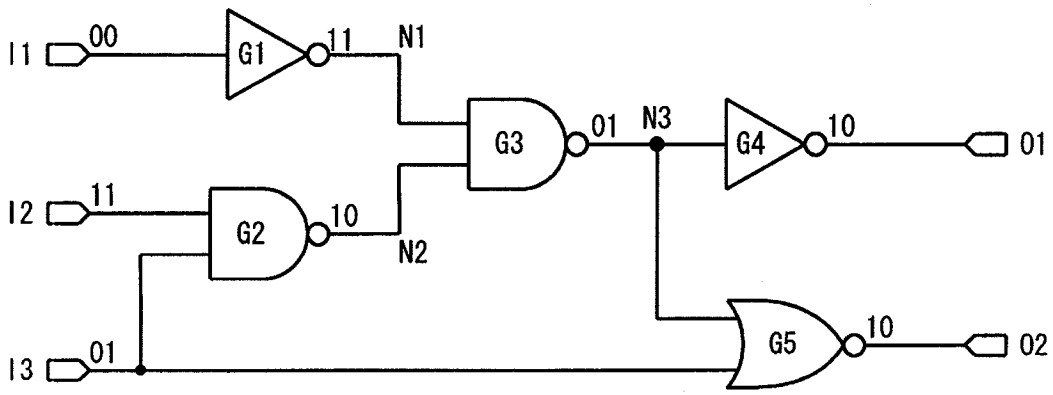


FIG. 14

TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL NODE			OUTPUT TERMINAL		DETECTABLE FAULTY GATE
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	G5
T2	0	1	R	1	F	R	F	F	G2, G3, G4, G5
T3	1	0	R	0	1	1	0	0	——
T4	1	1	R	0	F	1	0	0	G2
T5	0	R	0	1	1	0	1	1	——
T6	0	R	1	1	F	R	F	0	G2, G3, G4
T7	1	R	0	0	1	1	0	0	——
T8	1	R	1	0	F	1	0	0	G2
T9	R	0	0	F	1	R	F	F	G1, G3, G4, G5
T10	R	0	1	F	1	R	F	0	G1, G3, G4
T11	R	1	0	F	1	R	F	F	G1, G3, G4, G5
T12	R	1	1	F	0	1	0	0	G1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 15

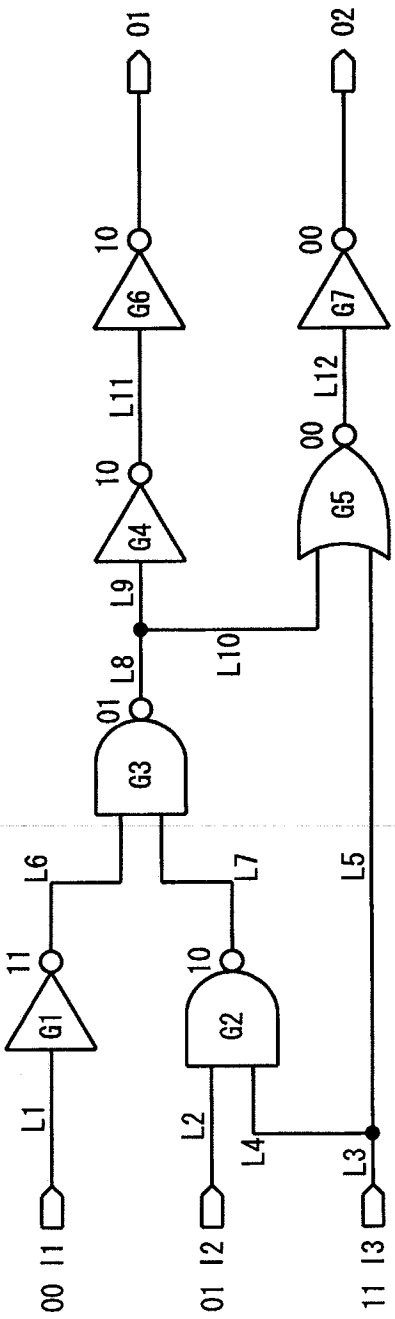

O1
O2
10
00
G6
G7
L11
L12
10
00
G4
G5
L9
L10
L8
01
G3
L6
L7
L5
11
10
G1
G2
L1
L2
L4
L3
00 I1
01 I2
11 I3

FIG. 16

TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL SIGNAL LINE												OUTPUT TERMINAL		DETECTABLE DEFECTIVE INTERNAL SIGNAL LINE
	I1	I2	I3	1	2	3	4	5	6	7	8	9	10	11	12	O1	O2	
T1	0	0	R	0	0	R	R	R	1	1	1	1	1	1	F	1	F	L3, L5, L12
T2	0	1	R	0	1	R	R	R	1	F	F	F	F	F	F	F	F	L3, L4, L5, L7, L8, L9, L10, L11, L12
T3	1	0	R	1	0	R	R	R	0	1	0	0	0	0	0	0	0	——
T4	1	1	R	1	1	R	R	R	0	F	0	0	0	0	0	0	0	L3, L4
T5	0	R	0	0	R	0	0	0	1	1	1	1	1	1	1	1	1	——
T6	0	R	1	0	R	1	1	1	1	F	F	F	F	F	0	F	0	L2, L7, L8, L9, L11
T7	1	R	0	1	R	0	0	0	0	1	0	0	0	0	0	0	0	——
T8	1	R	1	1	R	1	1	1	0	F	0	0	0	0	0	0	0	L2
T9	R	0	0	R	0	0	0	0	F	1	F	F	F	F	F	F	F	L1, L6, L8, L9, L10, L11, L12
T10	R	0	1	R	0	1	1	1	F	1	F	F	F	F	0	F	0	L1, L6, L8, L9, L11
T11	R	1	0	R	1	0	0	0	F	1	F	F	F	F	F	F	F	L1, L6, L8, L9, L10, L11, L12
T12	R	1	1	R	1	1	1	1	F	0	0	0	0	0	0	0	0	L1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 17

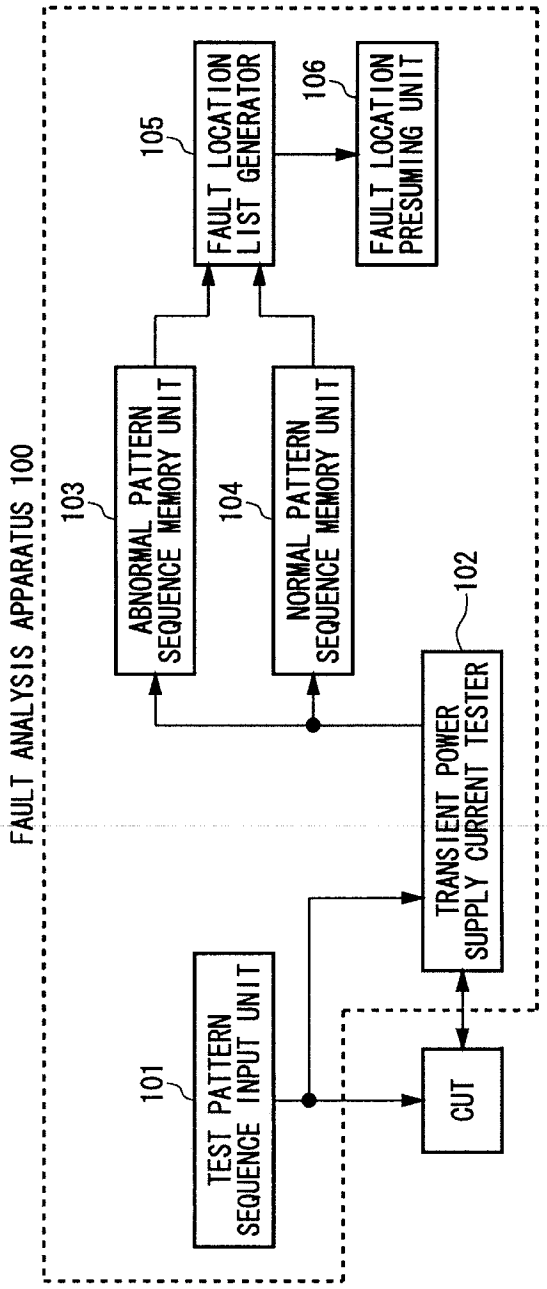

FAULT ANALYSIS APPARATUS 100
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
102
TRANSIENT POWER SUPPLY CURRENT TESTER
103
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
104
NORMAL PATTERN SEQUENCE MEMORY UNIT
105
FAULT LOCATION LIST GENERATOR
106
FAULT LOCATION PRESUMING UNIT

FIG. 18

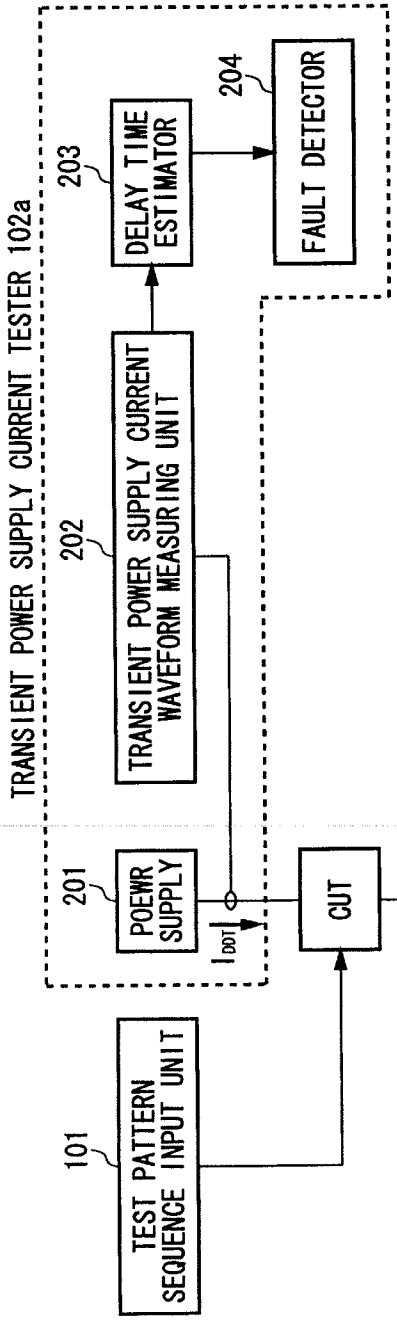

TRANSIENT POWER SUPPLY CURRENT TESTER 102a
101
TEST PATTERN SEQUENCE INPUT UNIT
201
POEWR SUPPLY
202
TRANSIENT POWER SUPPLY CURRENT WAVEFORM MEASURING UNIT
203
DELAY TIME ESTIMATOR
204
FAULT DETECTOR
CUT
GND
IDDT

FIG. 19

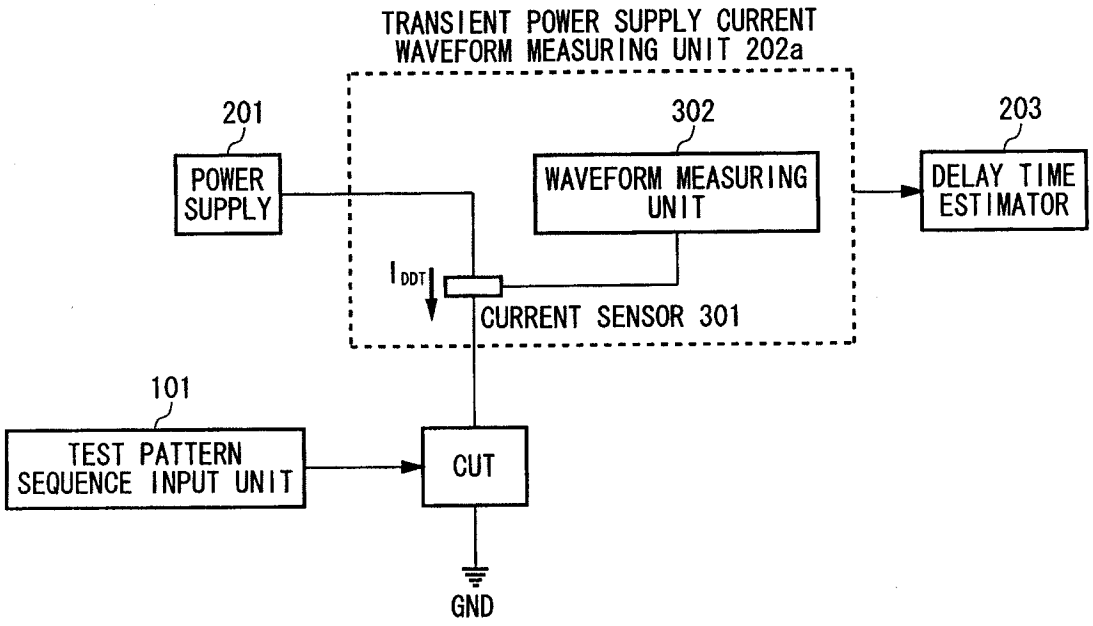

TRANSIENT POWER SUPPLY CURRENT
WAVEFORM MEASURING UNIT 202a
201
POWER SUPPLY
302
WAVEFORM MEASURING UNIT
203
DELAY TIME ESTIMATOR
I_{DDT}
CURRENT SENSOR 301
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 20

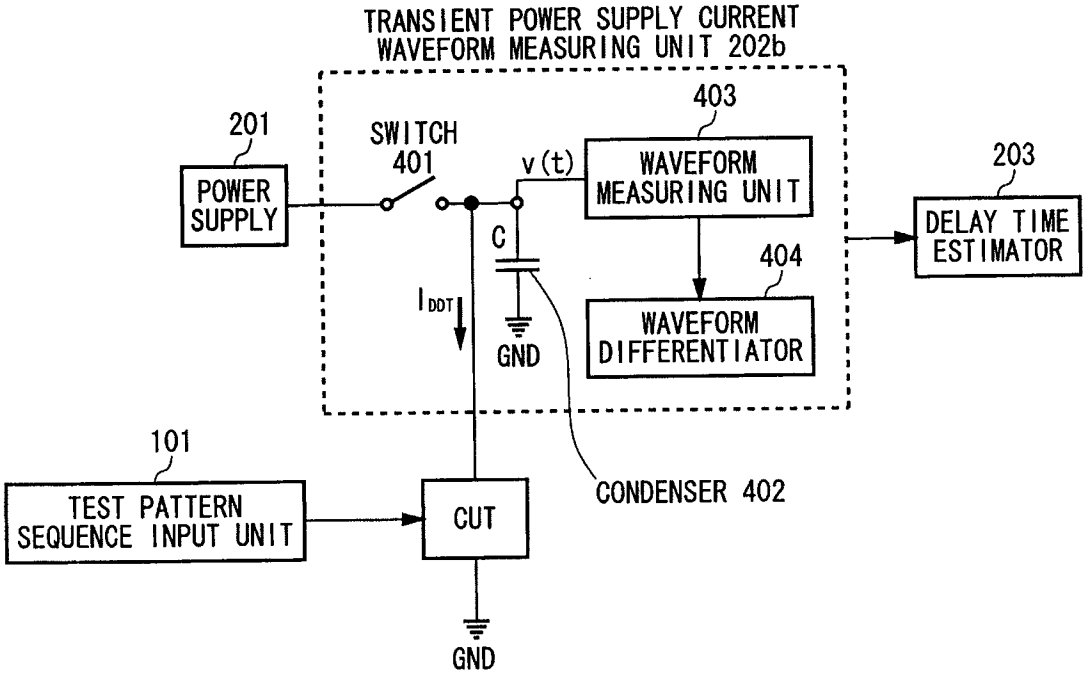

TRANSIENT POWER SUPPLY CURRENT
WAVEFORM MEASURING UNIT 202b
201
POWER SUPPLY
SWITCH
401
v(t)
403
WAVEFORM MEASURING UNIT
203
DELAY TIME ESTIMATOR
C
404
I_{DDT}
GND
WAVEFORM DIFFERENTIATOR
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
CONDENSER 402
GND

FIG. 21

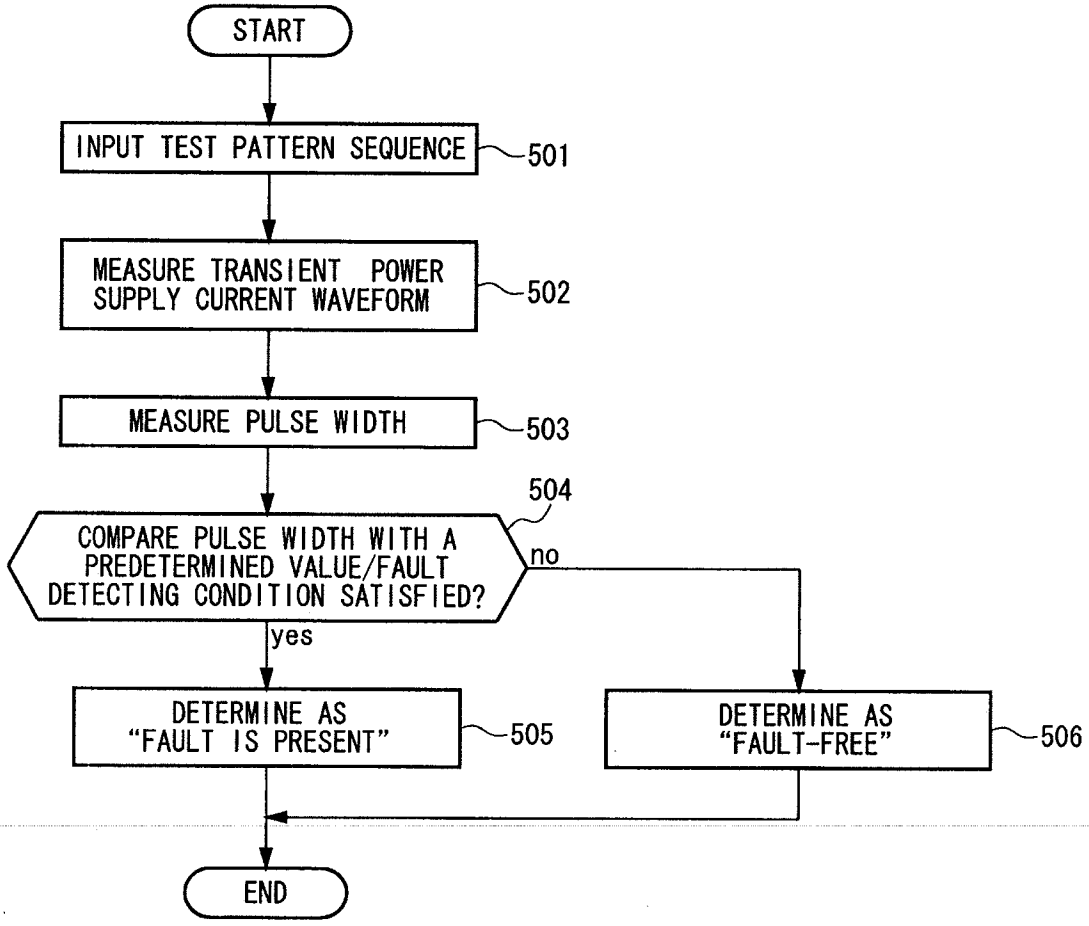

START
INPUT TEST PATTERN SEQUENCE
501
MEASURE TRANSIENT POWER SUPPLY CURRENT WAVEFORM
502
MEASURE PULSE WIDTH
503
504
COMPARE PULSE WIDTH WITH A PREDETERMINED VALUE/FAULT DETECTING CONDITION SATISFIED?
no
yes
DETERMINE AS "FAULT IS PRESENT"
505
DETERMINE AS "FAULT-FREE"
506
END

FIG. 22

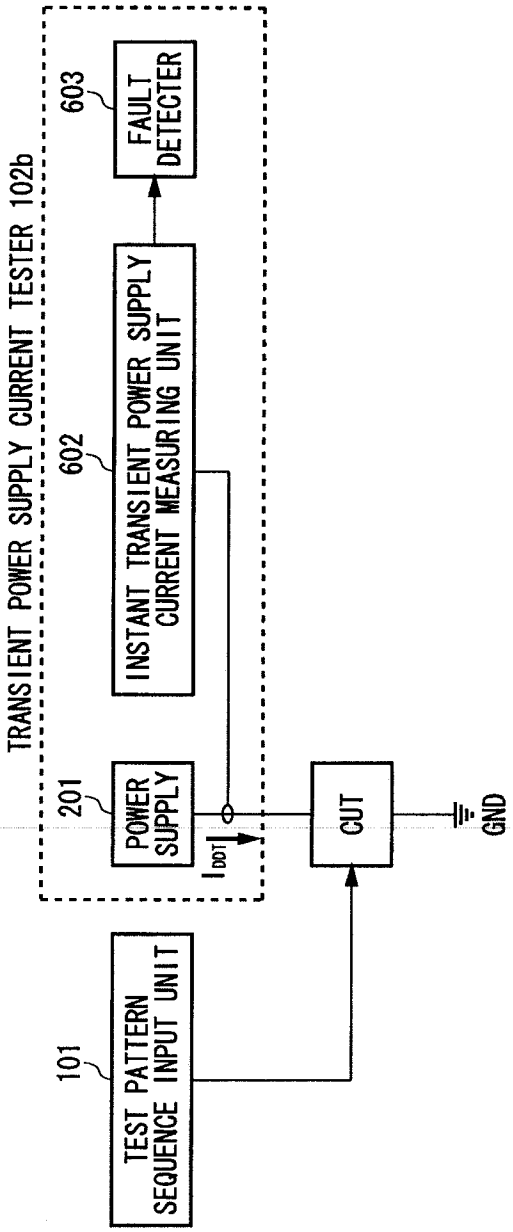

TRANSIENT POWER SUPPLY CURRENT TESTER 102b
603
FAULT DETECTER
602
INSTANT TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT
201
POWER SUPPLY
I_{DDT}
CUT
GND
101
TEST PATTERN SEQUENCE INPUT UNIT

FIG. 23

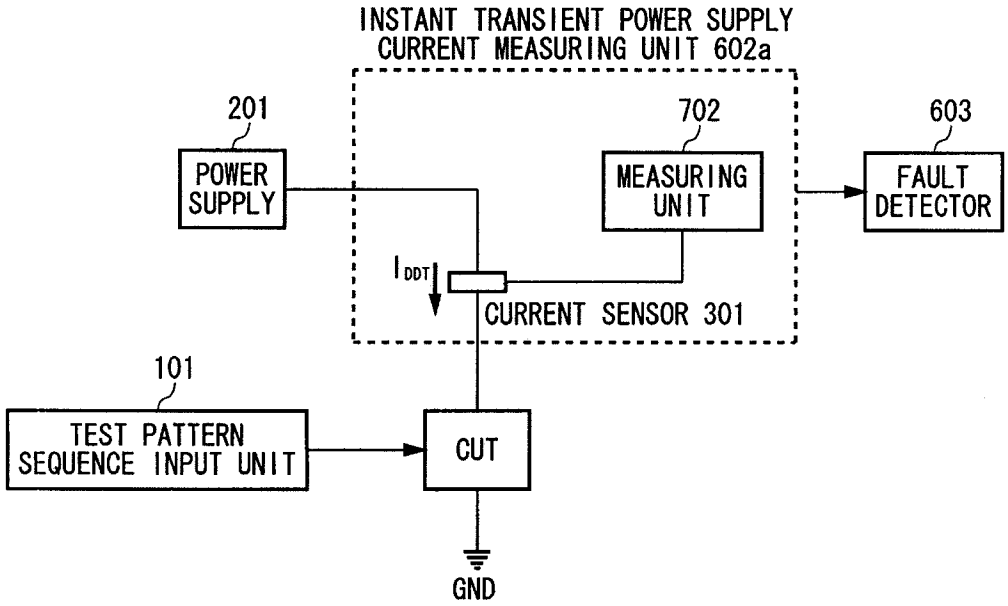

INSTANT TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 602a
201
POWER SUPPLY
702
MEASURING UNIT
603
FAULT DETECTOR
I_{DDT}
CURRENT SENSOR 301
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 24

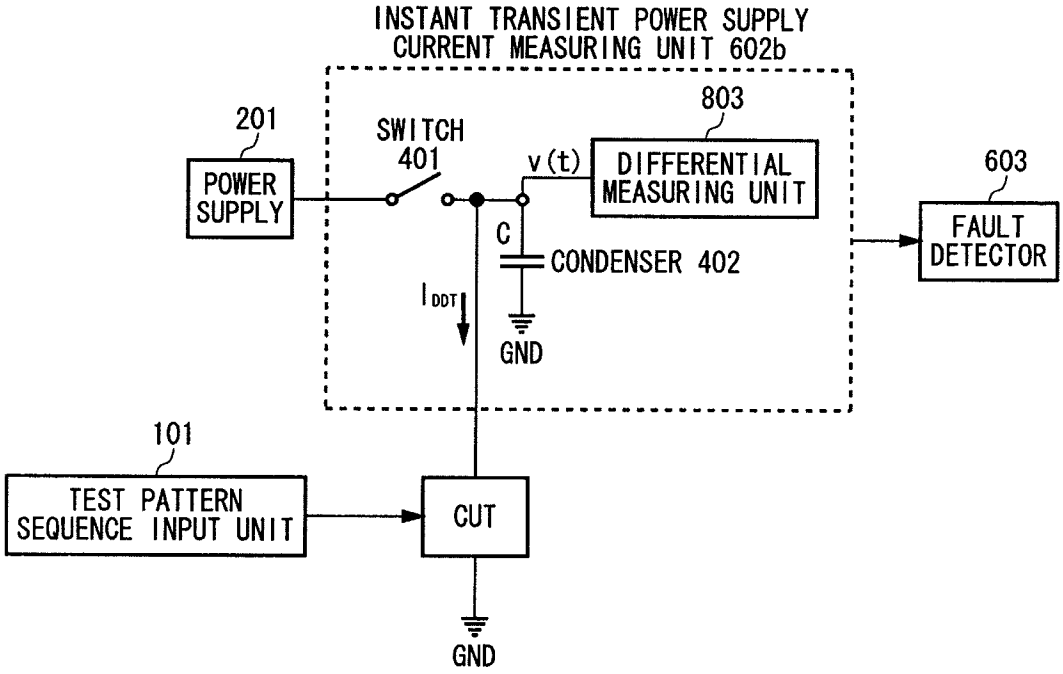

INSTANT TRANSIENT POWER SUPPLY
CURRENT MEASURING UNIT 602b
201
POWER SUPPLY
SWITCH
401
803
v(t)
DIFFERENTIAL MEASURING UNIT
603
FAULT DETECTOR
C
CONDENSER 402
I DDT
GND
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 25

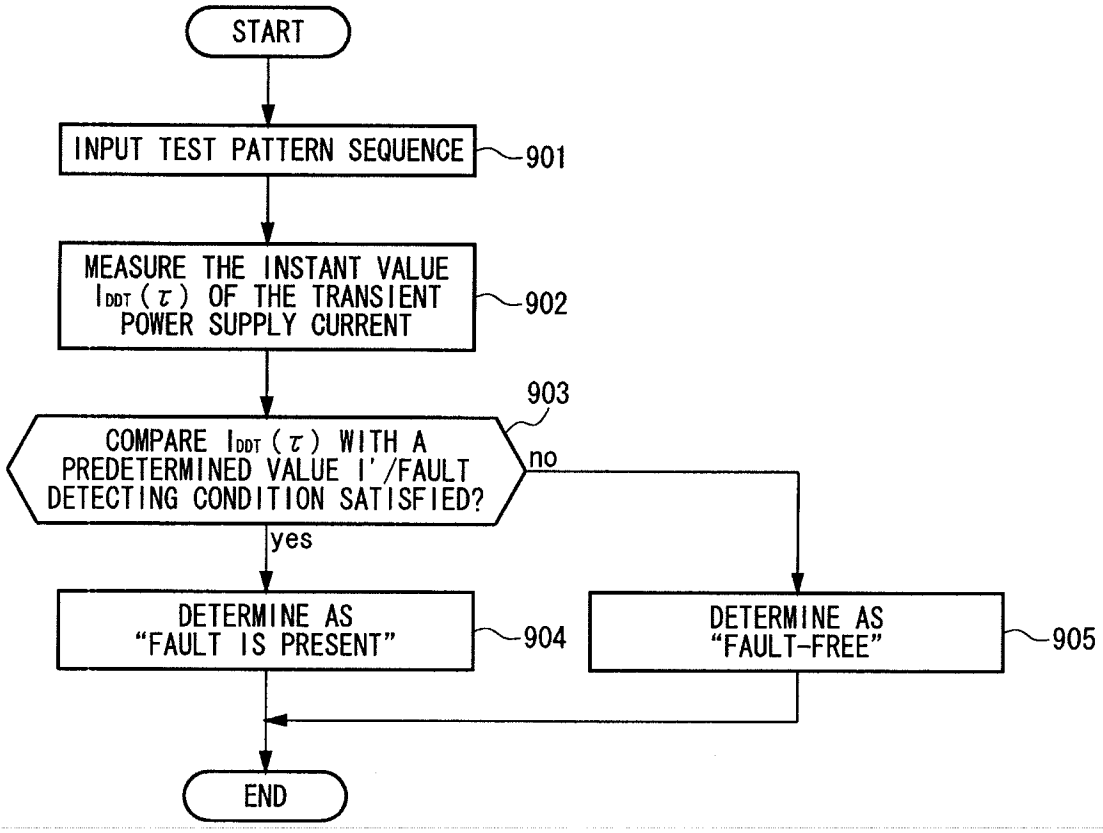

START
INPUT TEST PATTERN SEQUENCE
901
MEASURE THE INSTANT VALUE $I_{DDT}(\tau)$ OF THE TRANSIENT POWER SUPPLY CURRENT
902
903
COMPARE $I_{DDT}(\tau)$ WITH A PREDETERMINED VALUE I'/FAULT DETECTING CONDITION SATISFIED?
no
yes
DETERMINE AS "FAULT IS PRESENT"
904
DETERMINE AS "FAULT-FREE"
905
END

FIG. 26

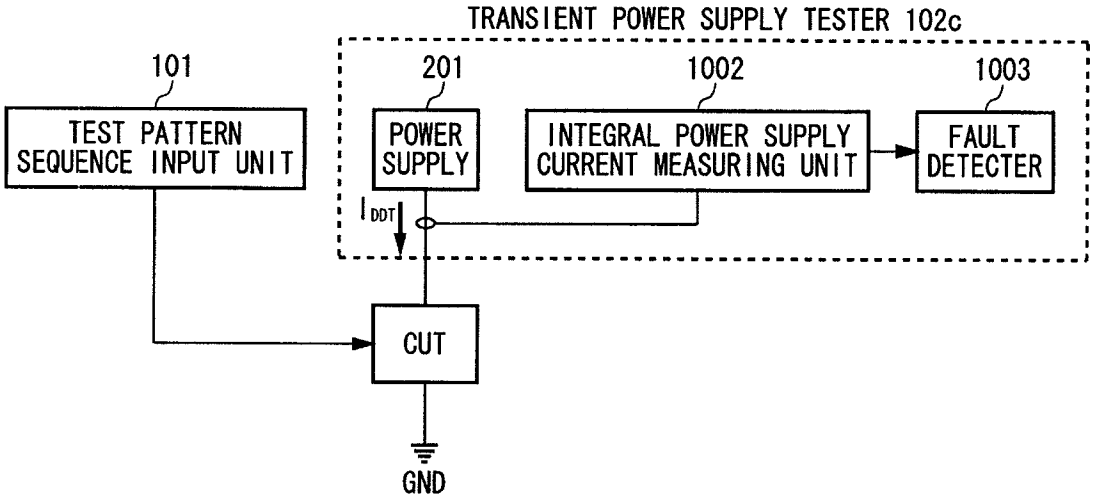

TRANSIENT POWER SUPPLY TESTER 102c
101
TEST PATTERN SEQUENCE INPUT UNIT
201
POWER SUPPLY
1002
INTEGRAL POWER SUPPLY CURRENT MEASURING UNIT
1003
FAULT DETECTER
I_{DDT}
CUT
GND

FIG. 27

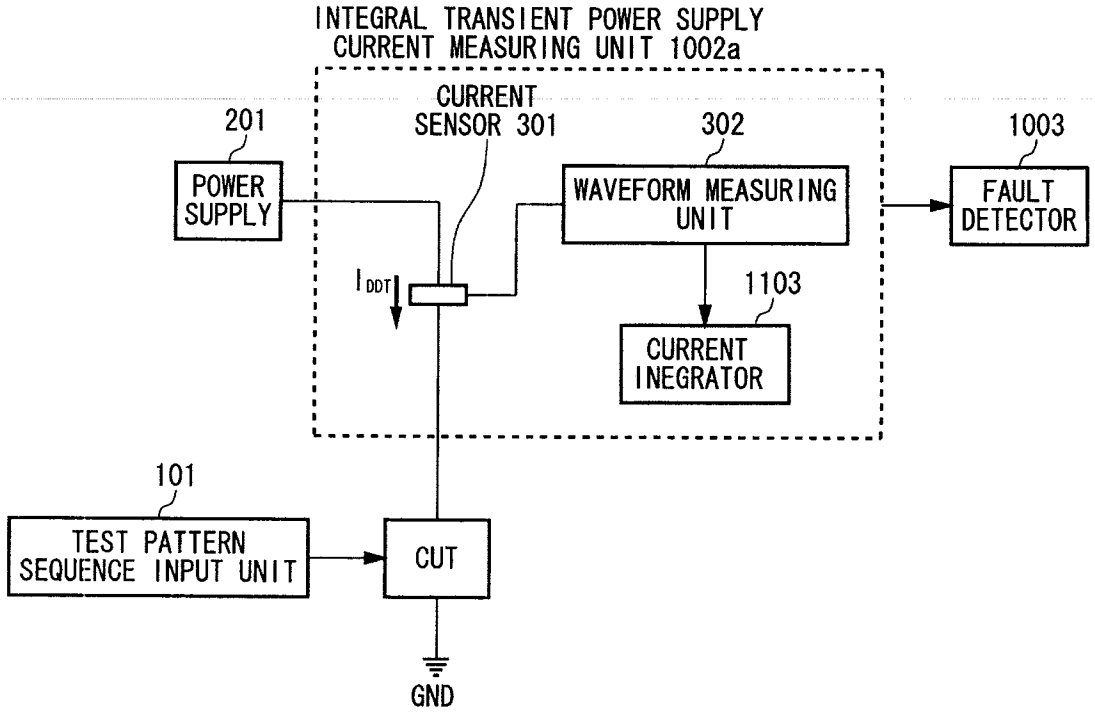

INTEGRAL TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 1002a
201
POWER SUPPLY
CURRENT SENSOR 301
302
WAVEFORM MEASURING UNIT
1003
FAULT DETECTOR
I_{DDT}
1103
CURRENT INEGRATOR
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 28

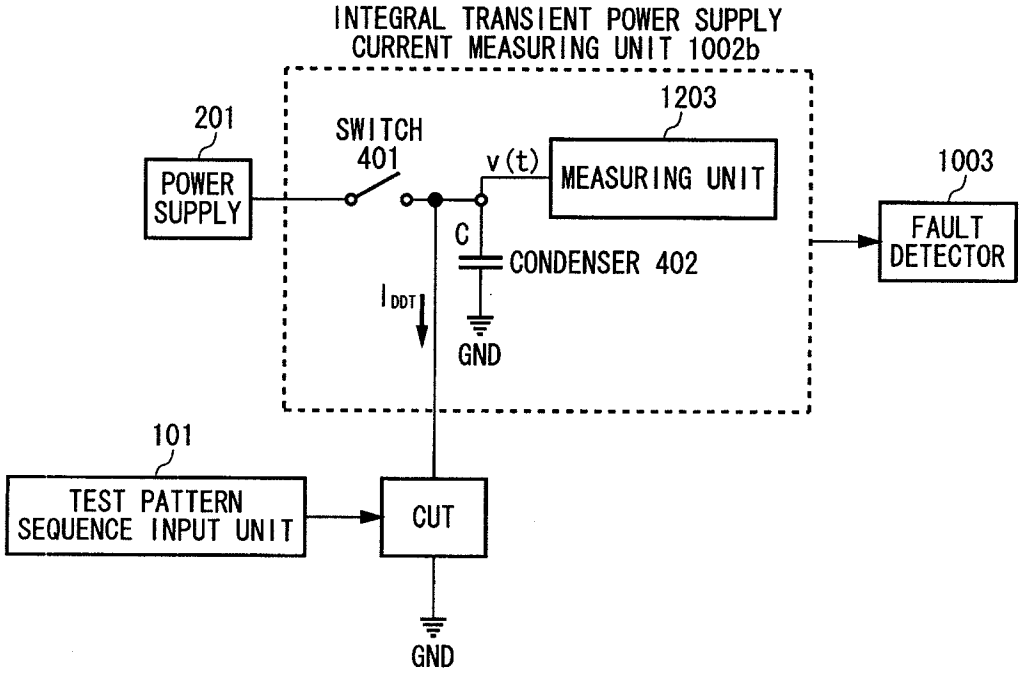

INTEGRAL TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 1002b
201
POWER SUPPLY
SWITCH 401
v(t)
1203
MEASURING UNIT
1003
FAULT DETECTOR
C
CONDENSER 402
I_{DDT}
GND
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 29

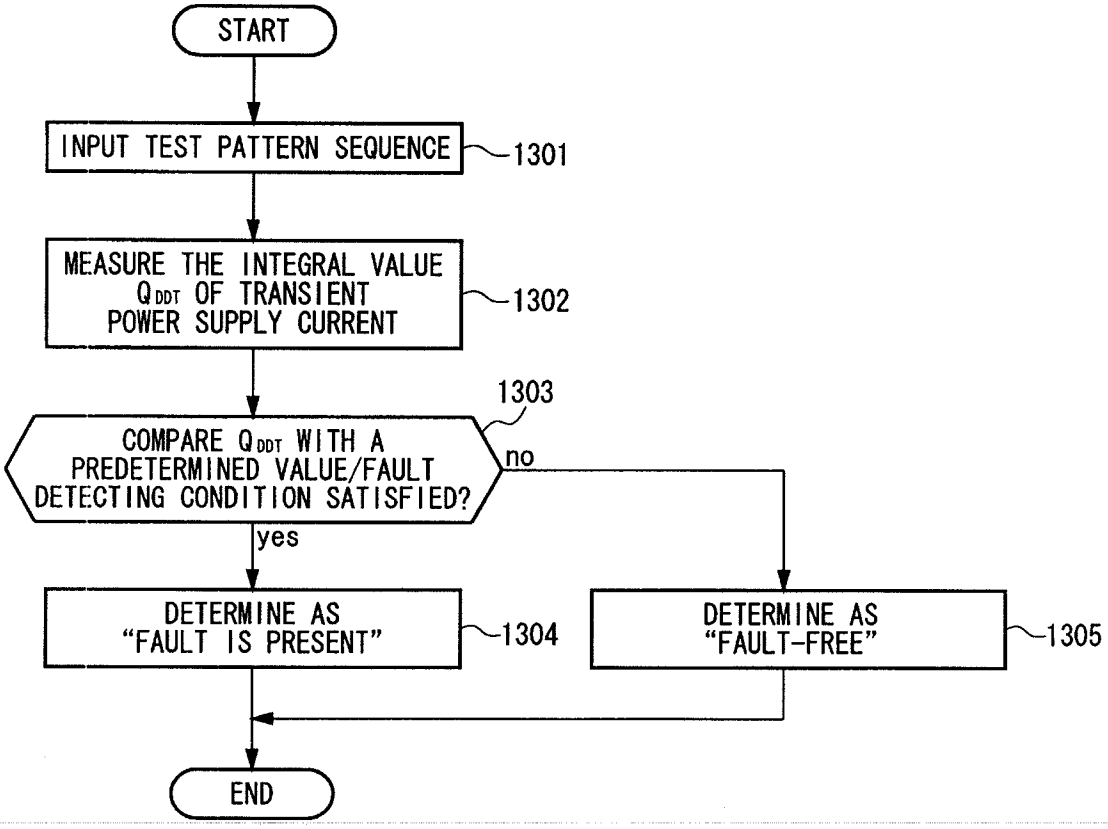

START
INPUT TEST PATTERN SEQUENCE
1301
MEASURE THE INTEGRAL VALUE Q_{DDT} OF TRANSIENT POWER SUPPLY CURRENT
1302
1303
COMPARE Q_{DDT} WITH A PREDETERMINED VALUE/FAULT DETECTING CONDITION SATISFIED?
no
yes
DETERMINE AS "FAULT IS PRESENT"
1304
DETERMINE AS "FAULT-FREE"
1305
END

FIG. 30

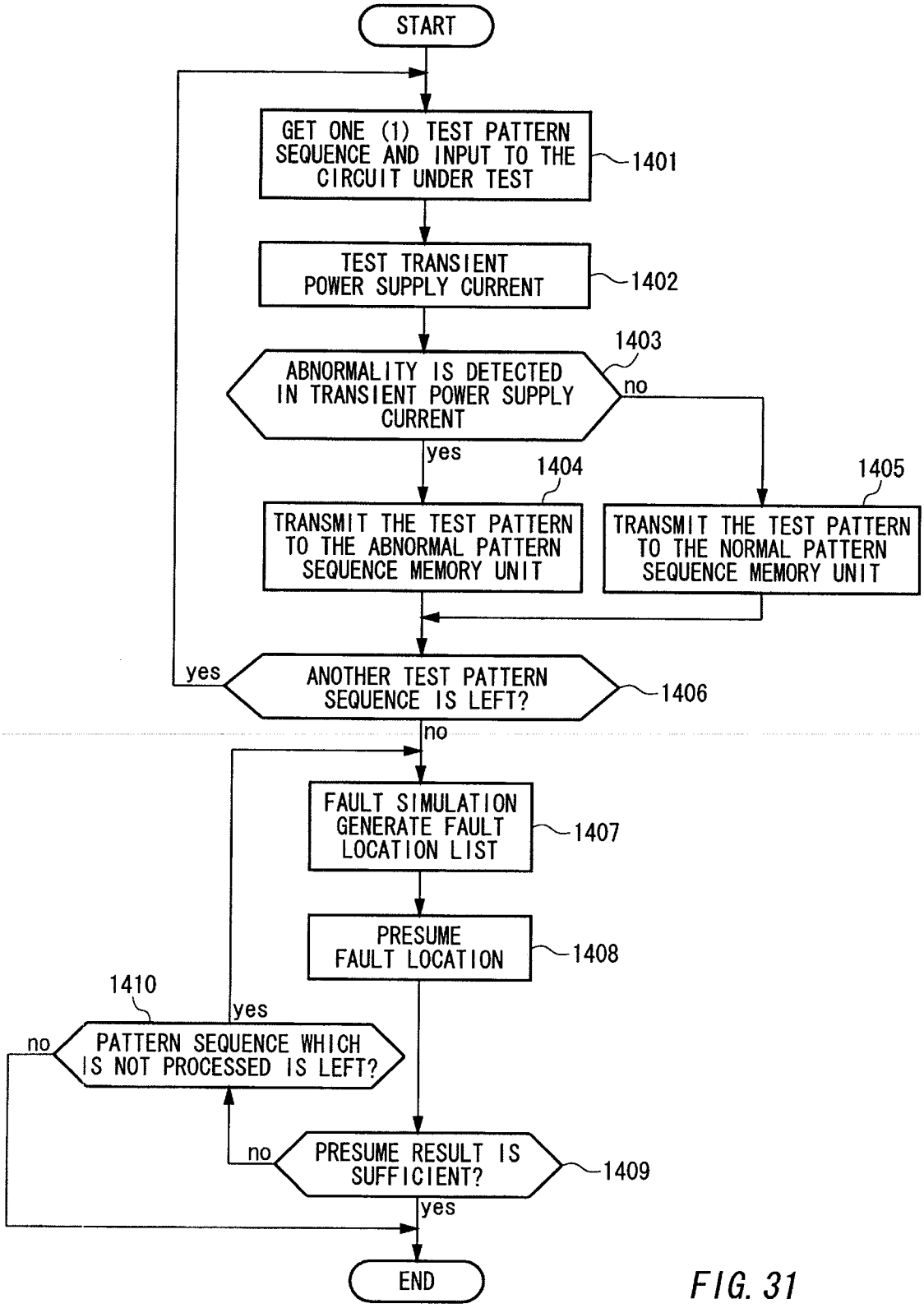

START
GET ONE (1) TEST PATTERN SEQUENCE AND INPUT TO THE CIRCUIT UNDER TEST
1401
TEST TRANSIENT POWER SUPPLY CURRENT
1402
1403
ABNORMALITY IS DETECTED IN TRANSIENT POWER SUPPLY CURRENT
no
yes
1404
TRANSMIT THE TEST PATTERN TO THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1405
TRANSMIT THE TEST PATTERN TO THE NORMAL PATTERN SEQUENCE MEMORY UNIT
yes
ANOTHER TEST PATTERN SEQUENCE IS LEFT?
1406
no
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1407
PRESUME FAULT LOCATION
1408
1410
yes
no
PATTERN SEQUENCE WHICH IS NOT PROCESSED IS LEFT?
no
PRESUME RESULT IS SUFFICIENT?
1409
yes
END

FIG. 31

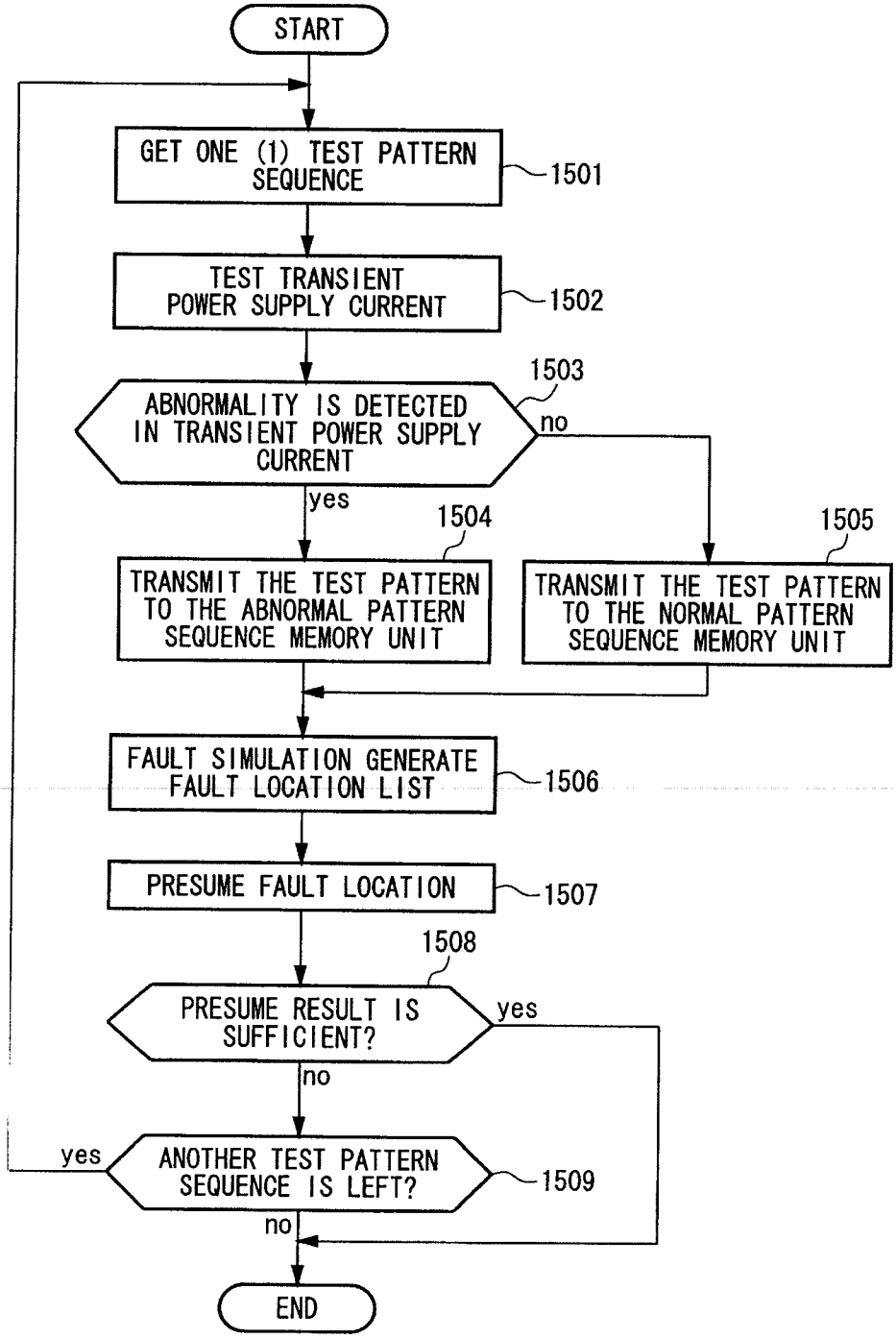

START
GET ONE (1) TEST PATTERN SEQUENCE
1501
TEST TRANSIENT POWER SUPPLY CURRENT
1502
1503
ABNORMALITY IS DETECTED IN TRANSIENT POWER SUPPLY CURRENT
no
yes
1504
TRANSMIT THE TEST PATTERN TO THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1505
TRANSMIT THE TEST PATTERN TO THE NORMAL PATTERN SEQUENCE MEMORY UNIT
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1506
PRESUME FAULT LOCATION
1507
1508
PRESUME RESULT IS SUFFICIENT?
yes
no
yes
ANOTHER TEST PATTERN SEQUENCE IS LEFT?
1509
no
END

FIG. 32

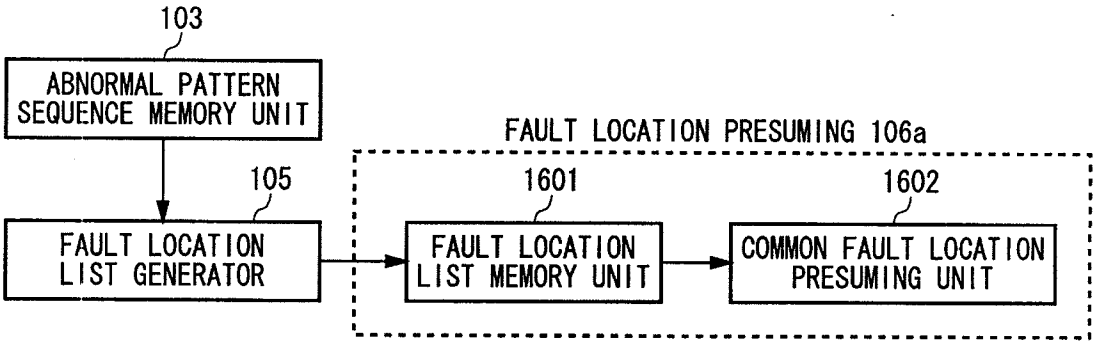

103
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
105
FAULT LOCATION LIST GENERATOR
FAULT LOCATION PRESUMING 106a
1601
FAULT LOCATION LIST MEMORY UNIT
1602
COMMON FAULT LOCATION PRESUMING UNIT

FIG. 33

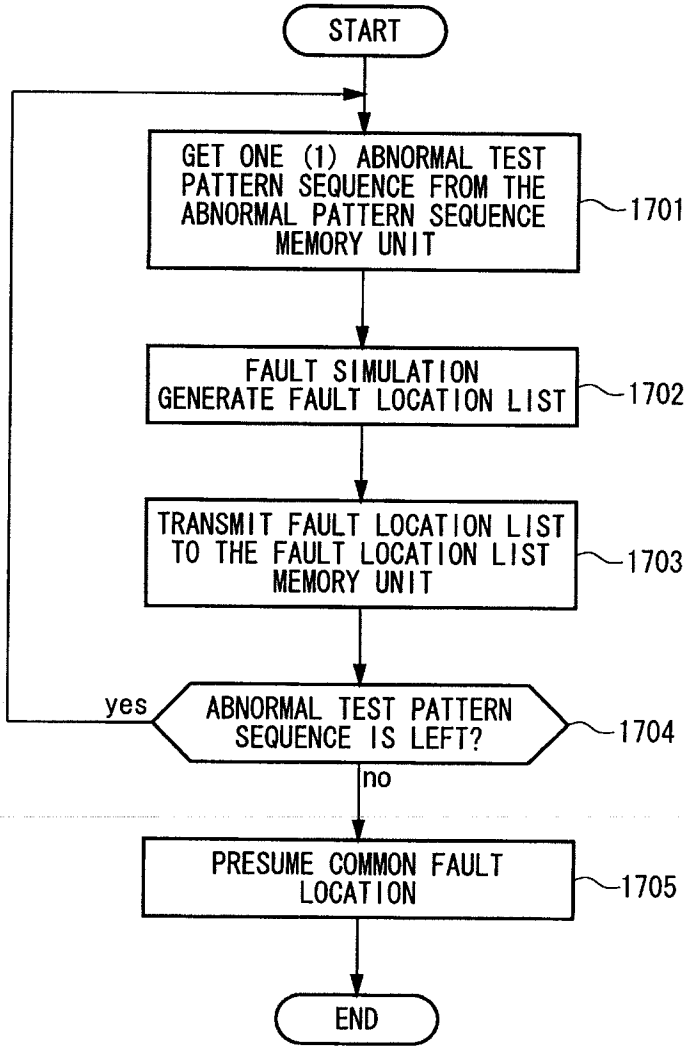

START
GET ONE (1) ABNORMAL TEST PATTERN SEQUENCE FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1701
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1702
TRANSMIT FAULT LOCATION LIST TO THE FAULT LOCATION LIST MEMORY UNIT
1703
yes
ABNORMAL TEST PATTERN SEQUENCE IS LEFT?
1704
no
PRESUME COMMON FAULT LOCATION
1705
END

FIG. 34

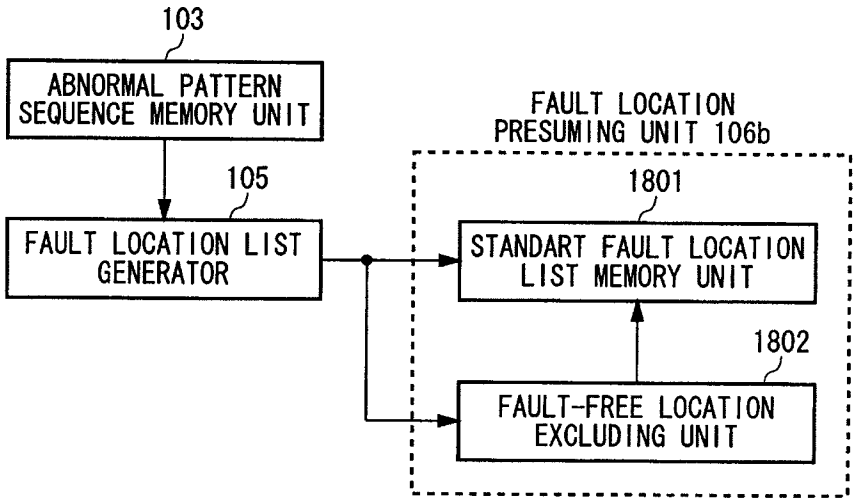

103
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
105
FAULT LOCATION LIST GENERATOR
FAULT LOCATION PRESUMING UNIT 106b
1801
STANDART FAULT LOCATION LIST MEMORY UNIT
1802
FAULT-FREE LOCATION EXCLUDING UNIT

FIG. 35

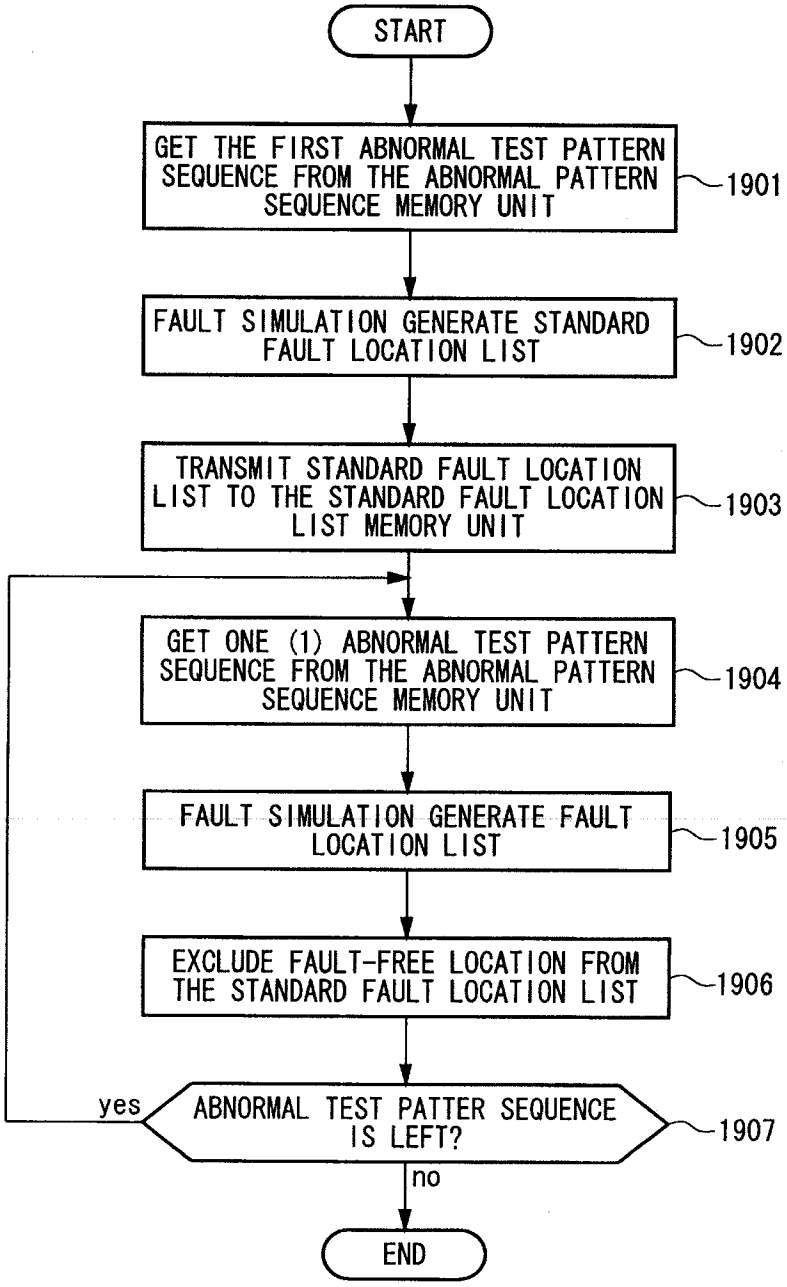

START
GET THE FIRST ABNORMAL TEST PATTERN SEQUENCE FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1901
FAULT SIMULATION GENERATE STANDARD FAULT LOCATION LIST
1902
TRANSMIT STANDARD FAULT LOCATION LIST TO THE STANDARD FAULT LOCATION LIST MEMORY UNIT
1903
GET ONE (1) ABNORMAL TEST PATTERN SEQUENCE FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1904
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1905
EXCLUDE FAULT-FREE LOCATION FROM THE STANDARD FAULT LOCATION LIST
1906
yes
ABNORMAL TEST PATTER SEQUENCE IS LEFT?
1907
no
END

FIG. 36

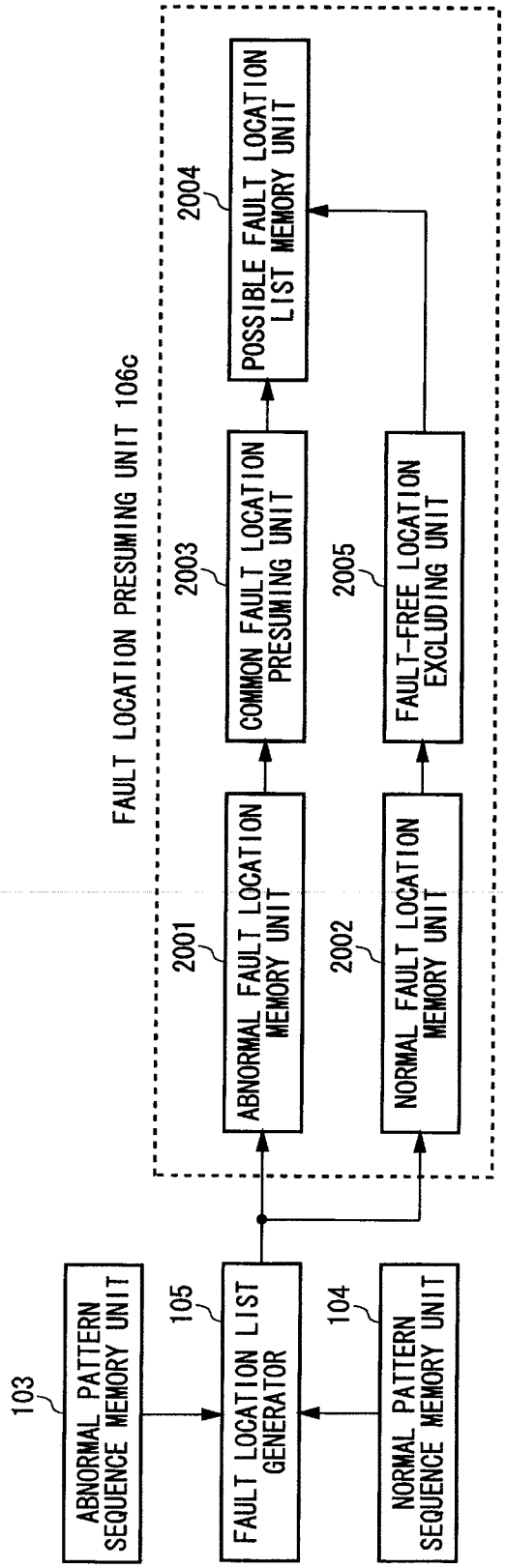

FAULT LOCATION PRESUMING UNIT 106c
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
103
FAULT LOCATION LIST GENERATOR
105
NORMAL PATTERN SEQUENCE MEMORY UNIT
104
ABNORMAL FAULT LOCATION MEMORY UNIT
2001
NORMAL FAULT LOCATION MEMORY UNIT
2002
COMMON FAULT LOCATION PRESUMING UNIT
2003
FAULT-FREE LOCATION EXCLUDING UNIT
2005
POSSIBLE FAULT LOCATION LIST MEMORY UNIT
2004

FIG. 37

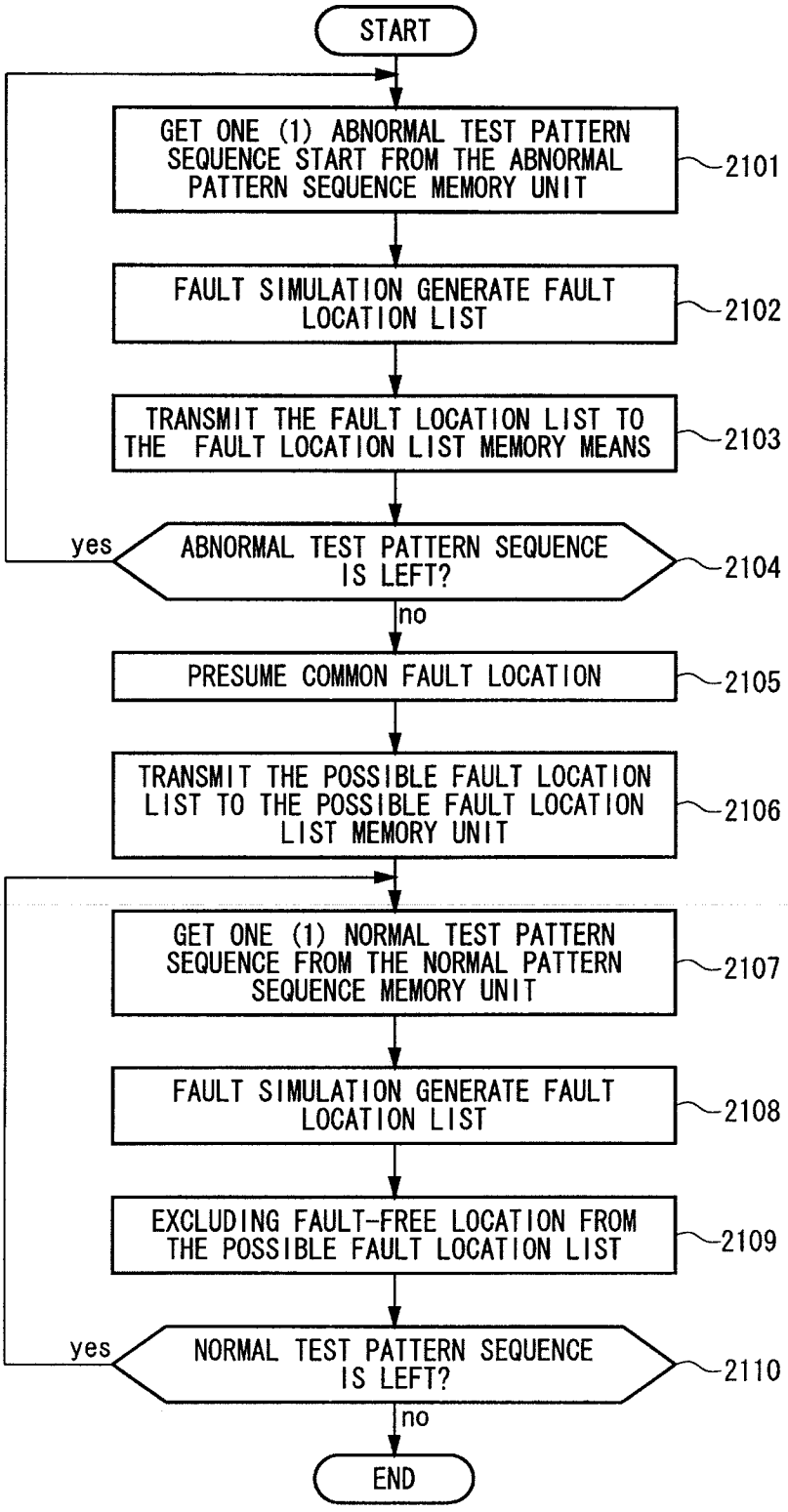

START
GET ONE (1) ABNORMAL TEST PATTERN SEQUENCE START FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
2101
FAULT SIMULATION GENERATE FAULT LOCATION LIST
2102
TRANSMIT THE FAULT LOCATION LIST TO THE FAULT LOCATION LIST MEMORY MEANS
2103
yes
ABNORMAL TEST PATTERN SEQUENCE IS LEFT?
2104
no
PRESUME COMMON FAULT LOCATION
2105
TRANSMIT THE POSSIBLE FAULT LOCATION LIST TO THE POSSIBLE FAULT LOCATION LIST MEMORY UNIT
2106
GET ONE (1) NORMAL TEST PATTERN SEQUENCE FROM THE NORMAL PATTERN SEQUENCE MEMORY UNIT
2107
FAULT SIMULATION GENERATE FAULT LOCATION LIST
2108
EXCLUDING FAULT-FREE LOCATION FROM THE POSSIBLE FAULT LOCATION LIST
2109
yes
NORMAL TEST PATTERN SEQUENCE IS LEFT?
2110
no
END

FIG. 38

TEST PATTERN SEQUENCE ID NO.	INPUT SIGNAL			INTERNAL NODE			OUTPUT TERMINAL		DETECTABLE FAULTY PATH
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	<I3, O2>
T2	0	1	R	1	F	R	F	F	<I3, N2, N3, O1> <I3, N2, N3, O2>
T3	1	0	R	0	1	1	0	0	——
T4	0	1	R	0	F	1	0	0	——
T5	0	R	0	1	1	0	1	1	——
T6	0	R	1	1	F	R	F	0	<I2, N2, N3, O1>
T7	1	R	0	0	1	1	0	0	——
T8	1	R	1	0	F	1	0	0	——
T9	R	0	0	F	1	R	F	F	<I1, N1, N3, O1> <I1, N1, N3, O2>
T10	R	0	1	F	1	R	F	0	<I1, N1, N3, O1>
T11	R	1	0	F	1	R	F	F	<I1, N1, N3, O1> <I1, N1, N3, O2>
T12	R	1	1	F	0	1	0	0	——
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 39

TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL SIGNAL LINE												OUTPUT TERMINAL		DETECTABLE FAULTY PATH
	I1	I2	I3	1	2	3	4	5	6	7	8	9	10	11	12	1	2	
T1	0	0	R	0	0	R	R	R	1	1	1	1	1	1	F	1	F	<I3, L3, L5, L12, 02>
T2	0	1	R	0	1	R	R	R	1	F	F	F	F	F	F	F	F	<I3, L3, L5, L12, 02> <I3, L3, L4, L7, L8, L9, L11, 01> <I3, L3, L4, L7, L8, L10, L12, 01>
T3	1	0	R	1	0	R	R	R	0	1	0	0	0	0	0	0	0	—
T4	1	1	R	1	1	R	R	R	0	F	0	0	0	0	0	0	0	—
T5	0	R	0	0	R	0	0	0	1	1	1	1	1	1	1	1	1	—
T6	0	R	1	0	R	1	1	1	1	F	F	F	F	F	F	F	0	<I2, L2, L7, L8, L9, L11, 01>
T7	1	R	0	1	R	0	0	0	0	1	0	0	0	0	0	0	0	—
T8	1	R	1	1	R	1	1	1	0	F	0	0	0	0	0	0	0	—
T9	R	0	0	R	0	0	0	0	F	1	F	F	F	F	F	F	F	<I1, L1, L6, L8, L9, L11, 01> <I1, L1, L6, L8, L10, L12, 02>
T10	R	0	1	R	0	1	1	1	F	1	F	F	F	F	0	F	0	<I1, L1, L6, L8, L9, L11, 01>
T11	R	1	0	R	1	0	0	0	F	1	F	F	F	F	F	F	F	<I1, L1, L6, L8, L9, L11, 01> <I1, L1, L6, L8, L10, L12, 02>
T12	R	1	1	R	1	1	1	1	F	0	0	0	0	0	0	0	0	—
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 40